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A comparative analysis of 128 bytes SRAM architecture using Single ended three and six transistor SRAM cells

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Abstract: *Static RAM architecture is an important part in the digital data processing devices like DSP's Micro Processors and Embedded systems for general purpose or specific purpose applications. Demand of manufacturing compact devices are increasing day by day, to make the compact devices the design of internal circuits area also should be reduced. This will in turn reduces the overall size of the device. In this paper two 128 bytes SRAM architectures are implemented with conventional six transistors SRAM cell and single ended three transistor SRAM cell from the scratch to layout level. The designs are compared in terms of power consumption, area, and speed with 45nm technology. The implemented design area is reduced by 57.14% with 92.37% reduced power consumption and with 89.98% improved performance.*

Key Word*: 128 bytes SRAM memory; SRAM architecture; single ended layout architecture; 128 bytes full-custom SRAM architecture; single ended SRAM architecture*

I. Introduction

The main aim of this paper is to compare two different designs of 128 bytes SRAM architectures in schematic and layout level. Design of SRAM architectures are very important to deal with cache memory. Cache memory is a kind of memory which is used to store frequently used data as well as a data processing RAM depending on requirement. Now-a- days SRAMS are replaced with DRAM as main memory because of its area constraint. But still there is a possibility to use SRAM as main memory if the number of transistors is reduced in the overall architecture. In the design of SRAM architectures apart from six transistors [1],[2],[3],[4] and [5] eight [6] nine [7] and ten [8] and [9] transistors are used for achieving good performance in various parameters like write stability, good readability, improved noise margins, less power consumption, high speed etc., by introducing various techniques. But six transistors SRAM is standard to compare any improved version of architectures. In this paper a comparison analysis taken place with standard six transistor SRAM and single ended three transistor SRAM architectures and stated the analysis of various parameters like transistor count, area, speed, power consumption, readability and write ability.

The paper is organized as follows: Chapter I introduction, Chapter II includes introduction of basic cells of SRAM architecture Chapter III includes design and implementation of one bit, one byte and 128 bytes architectures with three and six transistors SRAM cells, Chapter IV includes simulation analysis and comparison and Chapter V includes Conclusion.

II. Basic memory cells of SRAM architecture

Six transistor SRAM cell:

The Six transistors SRAM cell [10] construction is shown in figure 1.

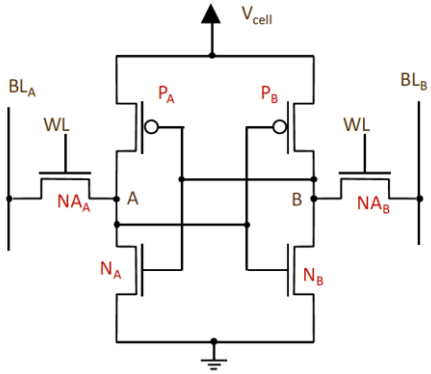

Figure no 1: six transistors Static RAM Cell.

To write digital data logic 1/0 in to the memory cell, the data 1/0 will be given to the data lines BL and BLB as actual data and inverted data respectively and the world line signal WL is enabled then the data 1/0 will be enter in to the points A and B respectively. After writing the data the WL signal will be disabled then the connecting points A and B are separated from BL and BLB respectively. The stored data will be read from the cell the WL signal is enabled again to provide the data from latch pints A and B to BL and BLB data lines respectively.

Three transistor SRAM cell:

Three transistors SRAM cells contain 2 NMOS logic pass transistors 1 PMOS logic pass transistor as shown in the figure 1. NMOS pass-transistor is connected to ground and PMOS pass-transistor is connected to supply voltage to provide full swing voltages to store logic 1 and 0. NMOS pass transistor is used to store or retrieve the data and separates the data stored point and bit line.

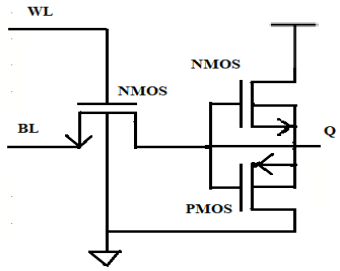

Figure no 2: Three transistor SRAM cell.

3 transistors SRAM cells working principle as follows:

Figure 2 show the combination of PMOS pass logic and NMOS pass logic in addition with one NMOS used to flow of data in and out. Read and write operations are taken place as explained above. For both in writing and reading operations the control signal BL is high during the operation. In write operation data will be stored at Q either 0 or 1 depending on the data that is given to input and control input signal WL high. In read operation data will be retrieved from Q either 0 or 1 depending on the data present which is already written in write operation at Q with the control input signal WL high and final output shows the full swing voltages.

III. Architectures design and implementation

The conventional 1 bit SRAM cell architecture usually consist 28 transistors. It comprises write driver, SRAM (6 transistor) cell, sense amplifier and pre-charge circuits. Three transistor 1 bit SRAM architecture is implemented with reduced write driver circuit, SRAM (3 transistor) cell and buffered output circuits. It consist total 12 transistors to store 1 bit of information. Approximately 60% area will be reduced so that speed will be increased and power consumption also will be reduced of the considerable value.

128 bytes SRAM archecture is implemented step by step from one bit, one byte to 128 bytes architecture. The designs are implemented in schematic and layout.

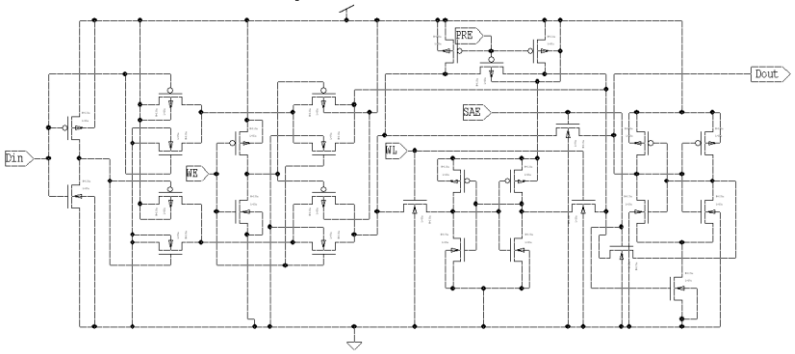

Figure no 3: Schematic: SRAM one bit architecture with 28 transistors.

Figure 3 shows the schematic design of one bit SRAM. It consist 28 transisotrs along with six transistor memory cell. The additional parts of the above diagram are write driver, pre-charge and sense amplifier circuits. In this diagram number of inputs and ouputs are 5 and 1 respectively. The layout construction of the same as shown in figure 4. The layout is implemented using 45nm technology. The total core area is 15.21 μm^2.

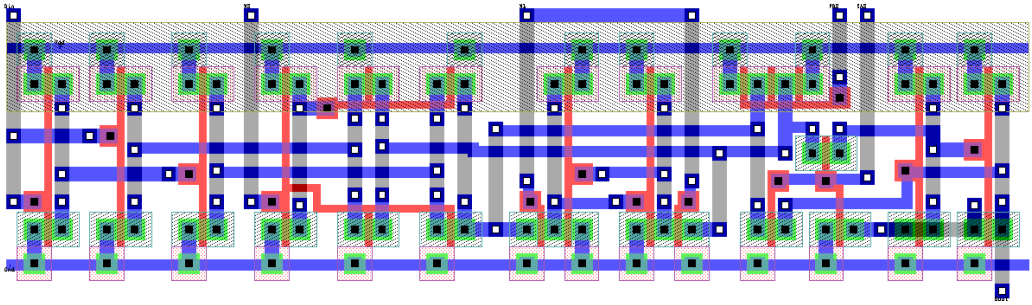

Figure no 4: Layout: SRAM one bit architecture with 28 transistors.

Figure 5 shows the schematic design of one byte SRAM. It consist 224 transisotrs with one bit SRAM transistor memory cell. Eight one bit SRAM cells are arranged in an array as one byte. It has eight data inputs, one read, one write enable one pre-charge, one word line enable inputs and eight data outputs. With control input signal eight bit data can be written in to the and read from the byte memory per operation. The layout construction of the same as shown in figure 6. The total core area is 222.91 μm^2.

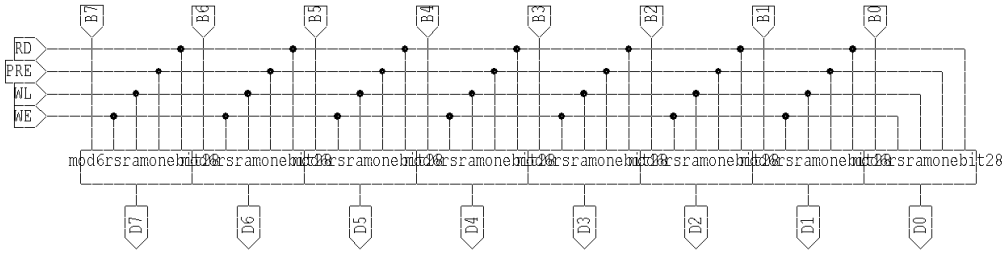

Figure no 5: Schematic: SRAM one byte architecture with 28 transistors SRAM cell.

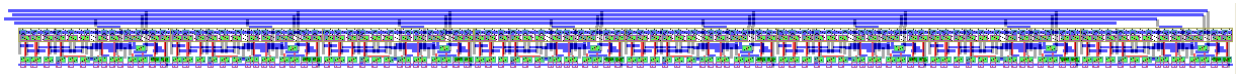

Figure no 6: Layout: SRAM one byte architecture with 28 transistors SRAM cell.

Figure 7 shows the schematic of 128 bytes SRAM architecture. It consist 28672 transisotrs with one byte SRAM memory cell. 128 one byte SRAM cells are arranged in an array as 128 bytes. It has eight data inputs, one read, one write one pre-charge, 128 address line enable inputs and eight data outputs. With control input signals eight bit data can be written in to and read from any one of the 128 bytes memory per operation. The 128 bytes memory is arranged in 16 columns and 8 rows. The layout construction of the same as shown in figure 8. The total core area is 38.65mm^2.

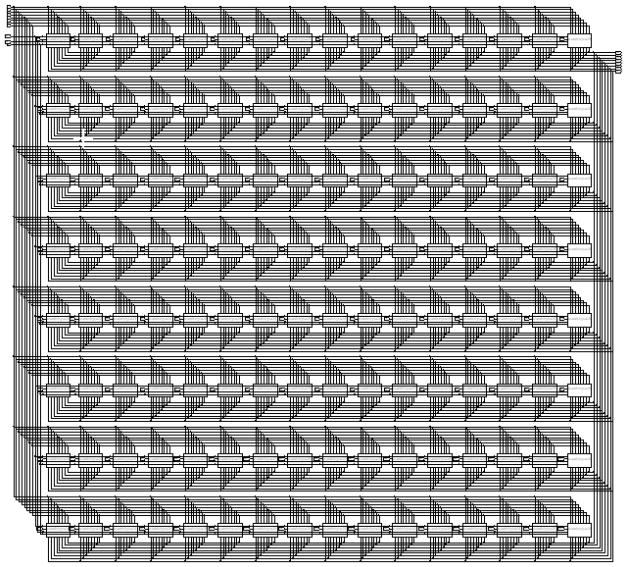

Figure no 7: Schematic: 128 bytes SRAM architecture with 28 transistors SRAM cell.

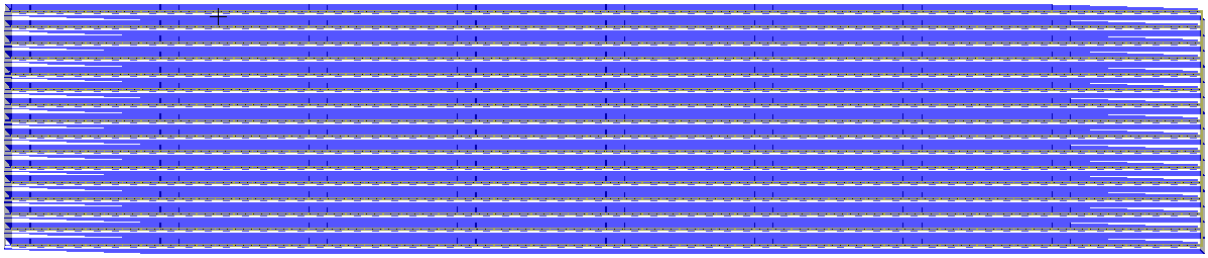

Figure no 8: Layout: 128 bytes SRAM architecture with 28 transistor SRAM cell.

Figure 9 shows the schematic of one bit SRAM. It consist 12 transisotrs along with three transistor memory cell. The additional parts of the above diagram are write driver and buffer amplifier circuits. In this diagram number of inputs and ouputs are 4 and 1 respectively. The layout construction of the same as shown in figure 10. The total core area is 5.25µm^2.

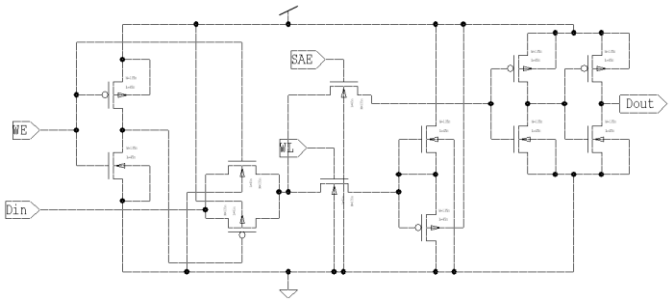

Figure no 9: Schematic: SRAM one bit architecture with 12 transistors.

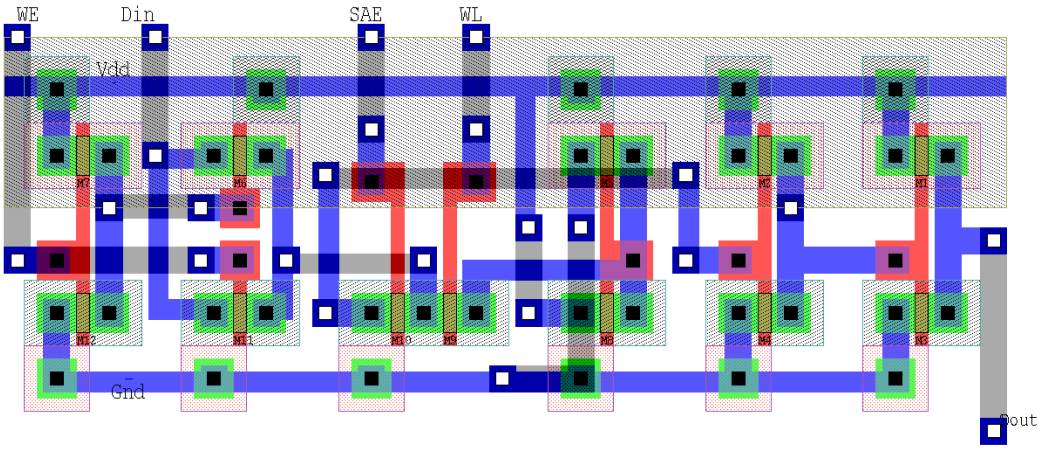

Figure no 10: Layout: SRAM one bit architecture with 12 transistors.

Figure 11 shows the schematic design of one byte SRAM. It consist 96 transisotrs with one bit SRAM transistor memory cell. Eight one bit SRAM cells are arranged in an array as one byte. It has eight data inputs, one read, one write enable one one word line enable inputs and eight data outputs. With control input signals eight bit data can be written in to and read from the byte memory per operation. The layout construction of the same as shown in figure 12. The total core area is 53.4µm^2.

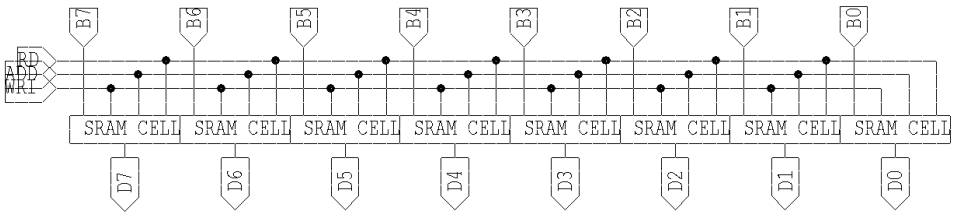

Figure no 11: Schematic: SRAM one byte architecture with 12 transistors.

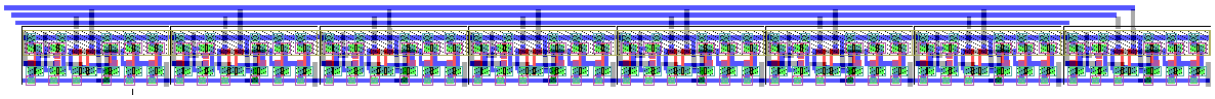

Figure no 12: Layout: SRAM one byte architecture with 12 transistors.

Figure 13 shows the schematic design of 128 bytes SRAM architecture. It consist 12288 transisotrs with one byte SRAM memory cell. 128 one byte SRAM cells are arranged in an array as 128 bytes . It has eight data inputs, one read, one write 128 address line enable inputs and eight data outputs. With control input signals eight bit data can be written in to and read from any one of the 128 bytes memory per operation. The 128 bytes memory is arranged in 8 columns and 16 rows. The layout construction of the same as shown in figure 14. The total core area is 18.76mm^2

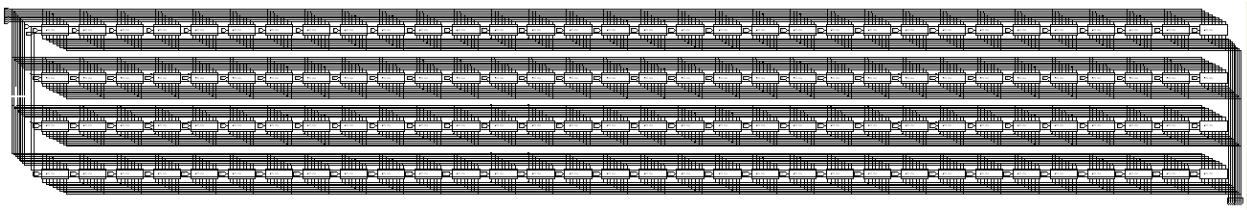

Figure no 13: Schematic: SRAM 128 bytes architecture with 12 transistors.

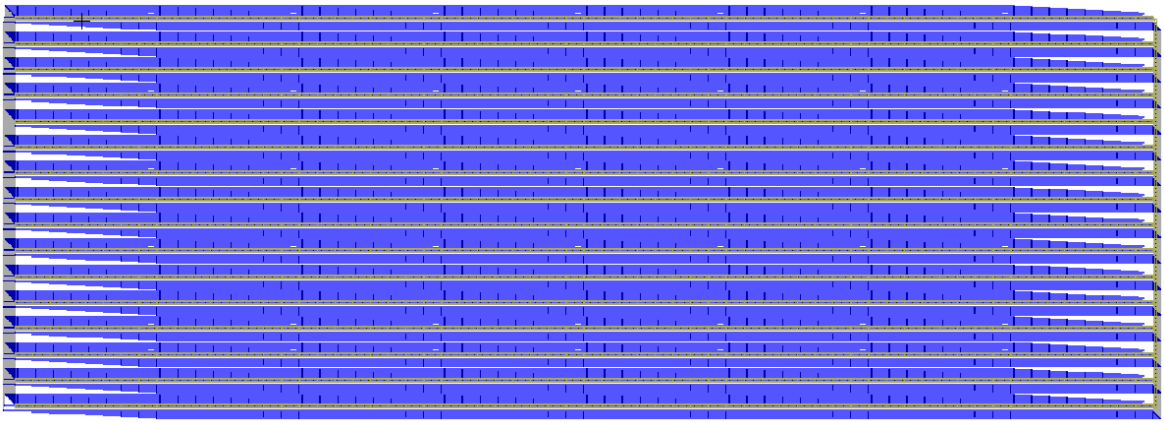

Figure no 14: Layout: SRAM 128 bytes architecture with 12 transistors.

IV. Simulation results and analysis

The simulation results of one bit, byte and 128 bytes SRAM architectures with 28 transistors and 12 transistors are shown in figures 15, 16, 17, 18, 19 and 20 respectively. All the designs are implemented in 45nm technology and simulated with 1V VDD. 10. Depending on address selection the corresponding SRAM cell will be active and gives the access to either to read or write the data. The data can be read or write based on its application like 8 bit, 16 bit, 32 bit etc., but the address will be allocated byte wise only.

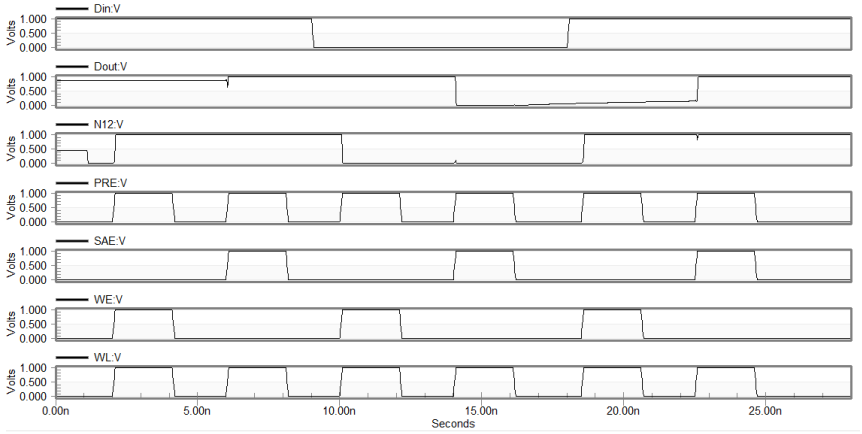

Figure no 15: Simulation results of one bit SRAM architecture with 28 transistors.

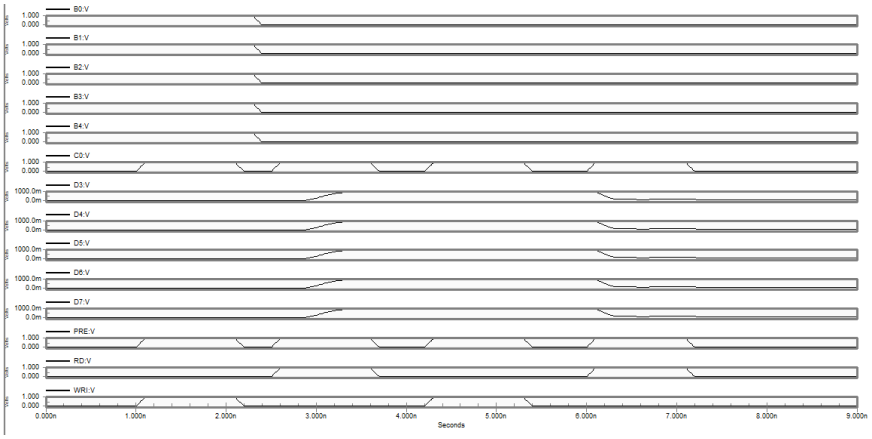

Figure no 16: Simulation results of one byte SRAM architecture with 28 transistors.

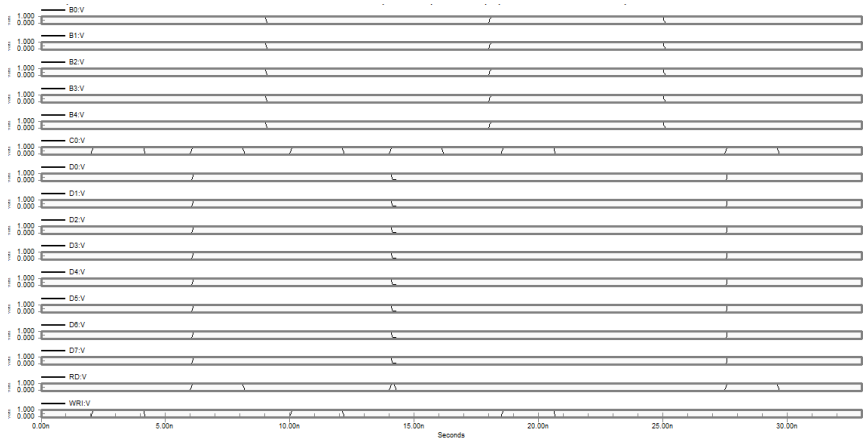

Figure no 17: Simulation results of 128 bytes SRAM architecture with 28 transistors.

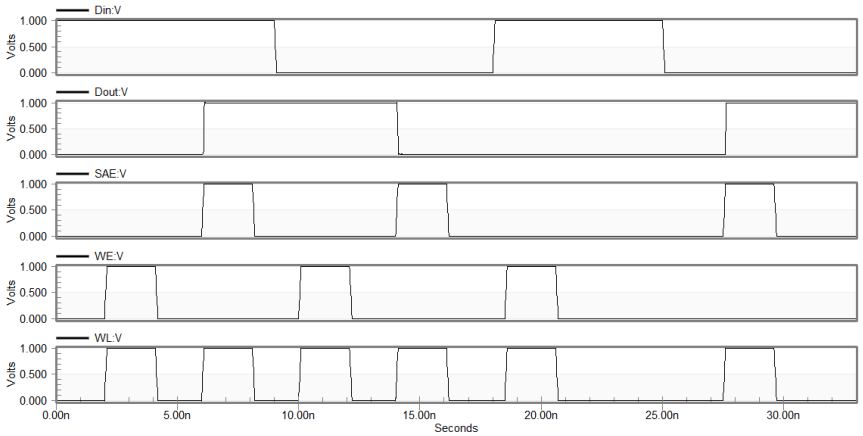

Figure no 18: Simulation results of one bit SRAM architecture with 12 transistors.

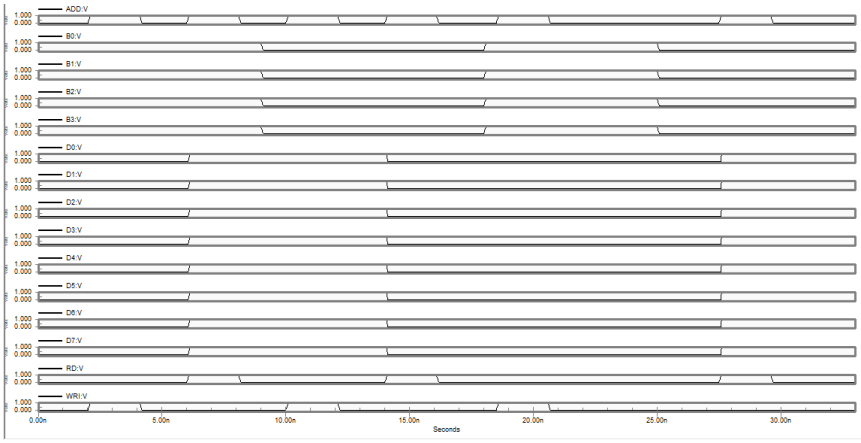

Figure no 19: Simulation results of one byte SRAM architecture with 12 transistors.

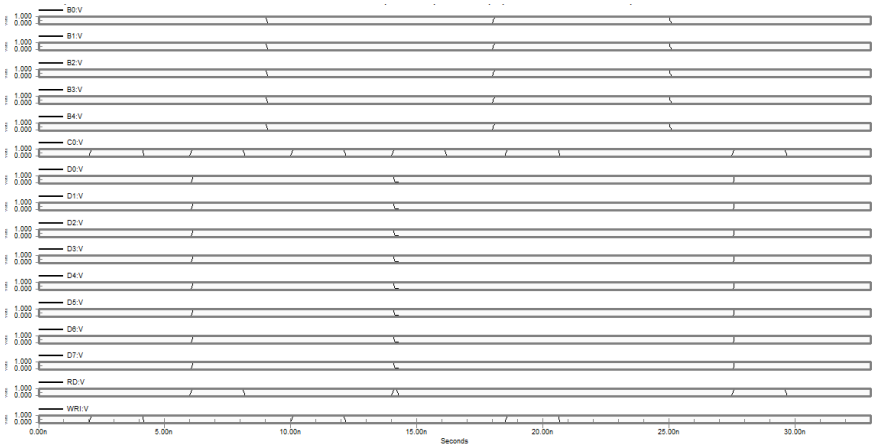

Figure no 20: Simulation results of 128 bytes SRAM architecture with 12 transistors.

In analysis the main parameters that are considered for comparison are average power, number of transistors and area and performance. The details are as follows.

Table 1 shows the average power consumption of one bit, byte and 128 bytes SRAM architectures with 28 and 12 transistors. 128 bytes SRAM architecture with 12 transistors average power consumption is reduced by 92.37% compared to 128 bytes SRAM architecture with 28 transistors.

Table no 1: Analysis of average power consumption

Sl.No	SRAM architectures	Avg. power consumption	
		With 28 transistors	With 12 transistors
1	One bit	1.29µW	7.07µW
2	One byte	14.7µW	24.4µW
3	128 bytes	43.6mW	3.3mW

Table 2 shows the number of transistors and area of one bit, byte and 128 bytes SRAM architectures with 28 and 12 transistors. 128 bytes SRAM architecture with 12 transistors transistor count is reduced by 57.14% and area is reduced by 51.46% compared to 128 bytes SRAM architecture with 28 transistors.

Table no 2: Analysis of transistor count and area

Sl.No.	SRAM architectures	With 28 transistors		With 12 transistors	
		Tr. count	Area	Tr. count	Area
1	One bit	28	15.21 μm^2	12	5.25 μm^2
2	One byte	224	222.9μm^2	96	53.4 μm^2
3	128 bytes	28672	38.65mm^2	12288	18.76mm^2

Table 3 shows the performance analysis of one bit, byte and 128 bytes SRAM architectures with 28 and 12 transistors. 128 bytes SRAM architecture with 12 transistors sustainably maintaining the performance irrespective of the size of memory compared to 128 bytes SRAM architecture with 28 transistors and the performance is increased by 89.98%.

Table no 3: Analysis of performance

Sl.No	SRAM architectures	Speed of operation	
		With 28 transistors	With 12 transistors
1	One bit	19.65GHz	18.68GHz
2	One byte	19.86GHz	18.76GHz
3	128 bytes	1.9GHz	18.98GHz

V. Conclusion

The design of bit, byte and 128 bytes schematics and layouts of 12 and 28 transistor architectures are implemented by using TANNER tool and the designs are verified by using TSPICE simulator with 45nm predictive technology model (PTM) file. Schematics are implemented by TANNER SEDIT and layouts implemented by TANNER LEDIT. All the designs are simulated properly and verified its outputs as per the respective operations. The implemented design area is decreased by 57.14% with 92.37% decreased power consumption and with 89.98% improved performance.

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