*Journal of Science and Technology*
*ISSN: 2456-5660 Volume 5, Issue 2, March-April 2020, PP 11-24*
*www.jst.org.in*

# Adaptive Neuro-Fuzzy Inference System (ANFIS) Based Nine Level Inverter fed PMSM Drive

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***Abstract:*** *Power electronic technology made possible to evolve inverter fed electric drives. The conventional Proportional-Integral (PI) speed control has been widely used in industrial motor controls due to its capabilities in controlling linear plants. However, motor behaves as non-linear plant where the PI speed control may not be able to provide precise speed responses. Permanent magnet synchronous motor (PMSM) is one motor replaced conventional electric motors with attractive features like compactness, lightweight and efficiency. The paper presents the Adaptive Neuro-Fuzzy Inference System (ANFIS) based nine-level diode clamped multi-level inverter fed PMSM. The fuzzy logic controller with rules-based is limited to a particular load torque due to its output membership functions, on the other hand, PI controller has better adaptability over load torque variation and has a smaller steady-state error even though it incurs the overshoot and has longer settling time. In this paper Nine-level diode clamped inverter is driven from pulse generator employing level-shifted (multi) carrier PWM pattern. Reference current signal is generated from closed-loop control of PMSM. Simulation work of the proposed concept is carried out and the results are presented using MATLAB/SIMULINK software.*

***Keywords*****:** *ANFIS, Disturbance observer, permanent-magnet synchronous motor (PMSM), Sliding-mode control (SMC), sliding-mode reaching law (SMRL).*

## I. Introduction

For many of the applications in agriculture and industries, use of motors to drive mechanical loads is been increased. Motor is used to reduce the human efforts when working with mechanical type of loads. Motor is a device which converts electrical energy to mechanical energy. Motors can be broadly classified as AC and DC motors. Use of commutator and brushes in DC motors pushes them back against other type of motors though they have good performance characteristics. Induction motors and synchronous motors are well known types of AC motors. Induction motor contains rotor coils and stator coils for its operation which eventually affects the power factor and increases the use of copper giving out losses with reduced efficiency of the system. Permanent magnet synchronous motor (PMSM) [1-4] is a synchronous motor uses only permanent magnets on its rotor and windings on its stator. Stator windings of PMSM are distributed winding and the back EMF (BEMF) is sinusoidal in shape [7-10]. No coils will be wounded on rotor circuit. This makes usage of PMSM in many applications over other type of motors [5-7]. Current flow in each winding (when excited) produces a magnetic field vector, which sums with the fields from the other windings. By controlling currents in the stator windings, a magnetic field of arbitrary direction and magnitude is produced by the stator. Torque is then produced by the attraction or repulsion between this net stator field and the magnetic field of the rotor. Conventional inverters give out square wave alternating output voltage consisting of high distortion. Alternating quantity with high distortion cannot be fed to any device and needs smoothing filters. Inverters are made up of capacitors and inductors which make the output current smooth as compared to switching square wave output we get with a conventional inverter. If the distortion quantity is high, filter size also increases. This phenomenon led to development of multi-level inverters [11-13].

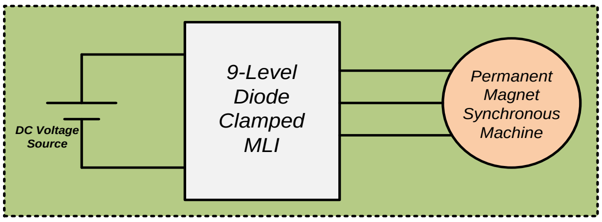


Figure 1: Representation of 9-level inverter fed PMSM

Multi-level inverters became the prior pick for high power high voltage applications. Multi-level inverters are able to generate high voltage with lower rated devices. Multi-level inverter generates leveled (stepped) output and as the number of level increases better output voltage waveform is obtained. Diode clamped multi-level inverters are one among multi-level topologies and uses diodes as clamping elements. Multi-level inverter driven PMSM is shown in figure 1. The paper presents the analysis of nine-level diode clamped multi-level inverter fed PMSM. Nine-level diode clamped inverter is driven from pulse generator employing level-shifted (multi) carrier PWM pattern. Reference current signal is generated from closed-loop control of PMSM.

## II. PERMANENT MAGNET SYNCHRONOUS MOTOR DRIVE

The motor drive consists of four main components, the PM motor, inverter, control unit and the position sensor. The components are connected as shown in Fig. 1

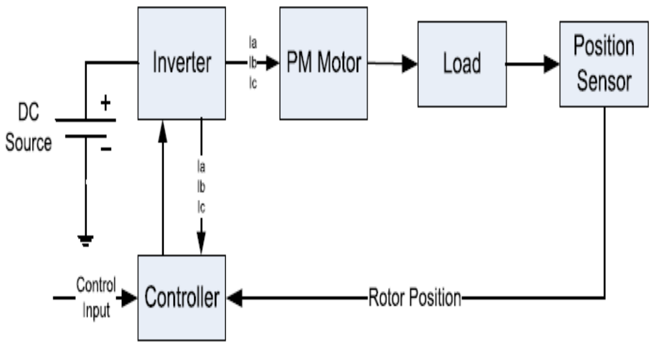


**Fig. 1 Drive System Schematic**

Descriptions of the different components are as follows

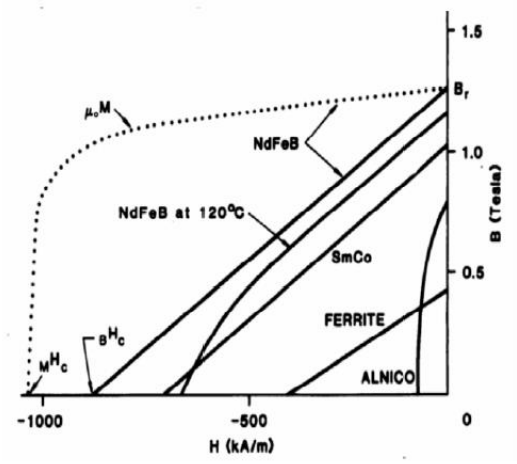


**Fig. 2 Flux Density versus Magnetizing Field of PMSM**

## III. PERMANENT MAGNETIC MATERIALS

The most punctual manufactured magnetic materials were solidified steel. The magnets made of steel have been effectively polarized. However, they may have had little vitality and it was far from difficult to demagnetize. In recent times other magnetic materials, for example aluminum compounds, nickel and cobalt (ALNICO), strontium or barium ferrite (ferrite), samarium cobalt (rare earth magnet of the first era) (SmCo) and iron-boron neodymium (rare earth magnet of the second era) (NdFeB) was created and used to create perpetual magnets.
Earth's uncommon magnets are classified into two classes: cobalt samarium magnets (SmCo) and iron boron neodymium magnets (NdFeB). SmCo magnets have higher transition thickness levels, but are excessively expensive. NdFeB magnets are the most common ground magnets most used in today's motors. A transition thickness is shown in Fig. 2 as opposed to the polarization field for these magnets.

## IV. NINE-LEVEL DIODE CLAMPED INVERTER FED PMSM DRIVE

The need of multilevel converter is to give a high output power from medium voltage source. Sources like batteries, super capacitors, solar panel are medium voltage sources. The multi level inverter consists of several switches. In the multi level inverter the arrangement switches' angles are very important. Multilevel inverters (MLI) are becoming increasingly popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion and lower electromagnetic interference. Multilevel inverters are capable of generating output voltage with very low harmonic distortion with low dv/dt.

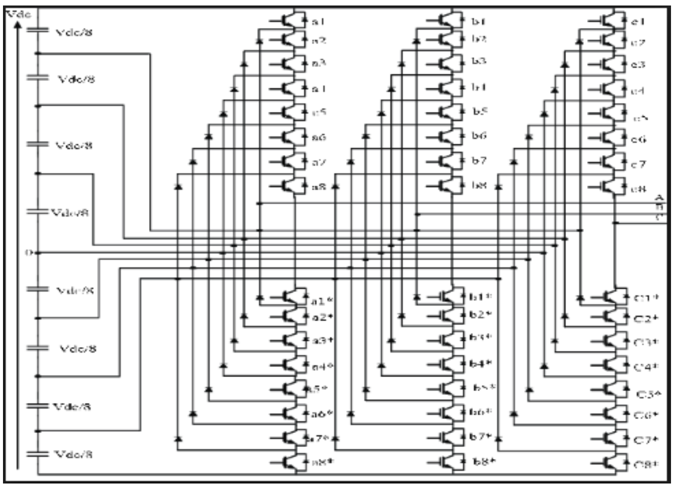

Figure 2: 9-level diode clamped inverter

Diode clamped MLI (DCMLI) shown in figure 2 or also called as neutral point clamped MLI is one of the topology of multi-level structure. DCMLI uses diodes and provides the multiple voltage levels through the different phases to the capacitor banks which are in series. A diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices. The maximum output voltage is half of the input DC voltage in DMLI.

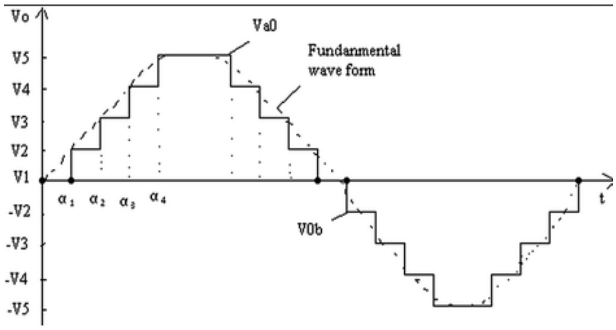


Figure 3: Output of 9-level DCMLI

Table-1: Switching pattern for 9-level DCMLI

| Volt | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A1* | A2* | A3* | A4* | A5* | A6* | A7* | A8* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| V9 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| V8 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| V7 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| V6 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| V5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| V4 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| V3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| V2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| V1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

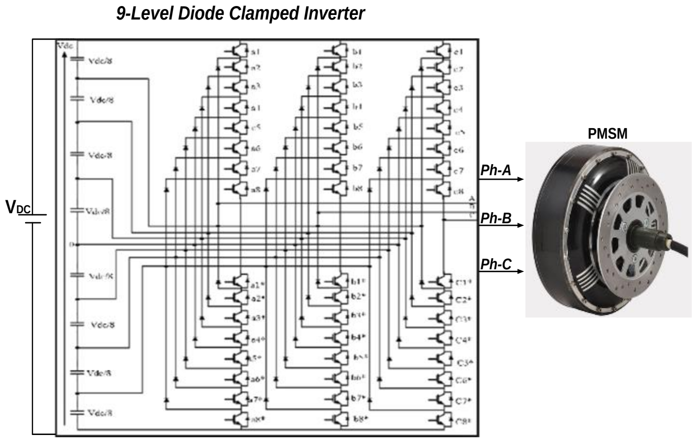


Figure 3 shows the output obtained from 9-level DCMLI and table-I shows switching pattern of 9-level DCMLI. Figure 4 shows the 9-level DCMLI fed PMSM.

## V. CONTROL STRATEGY

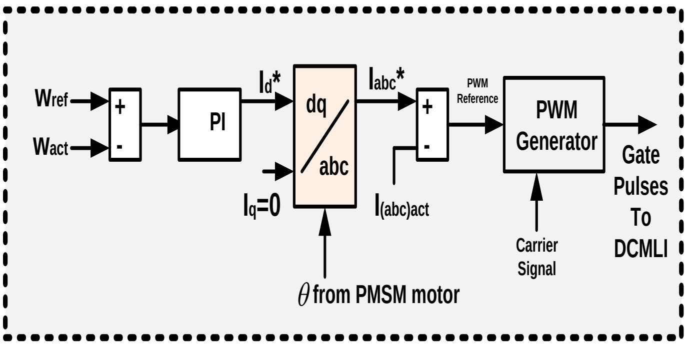


Figure 5: Speed control of PMSM fed from DCMLI

n speed control operation of PMSM drive, initially the actual speed of the PMSM is compared to reference speed value. Actual speed is measured by speed sensors. Error signal is sent to PI controller to obtain reference d-axis current. Reference q-axis current is considered to be zero. Then, 'dq' coordinates are transformed to 'abc' coordinates giving out reference current signal. The reference current signal obtained is compared to actual current from the PMSM which gives out the PWM reference signal. Relational operated PWM reference and carrier signals using LSCPWM pattern generated gate pulses to the diode clamped inverter. Figure 6 shows the complete schematic arrangement of 9-level DCMLI fed PMSM with control.

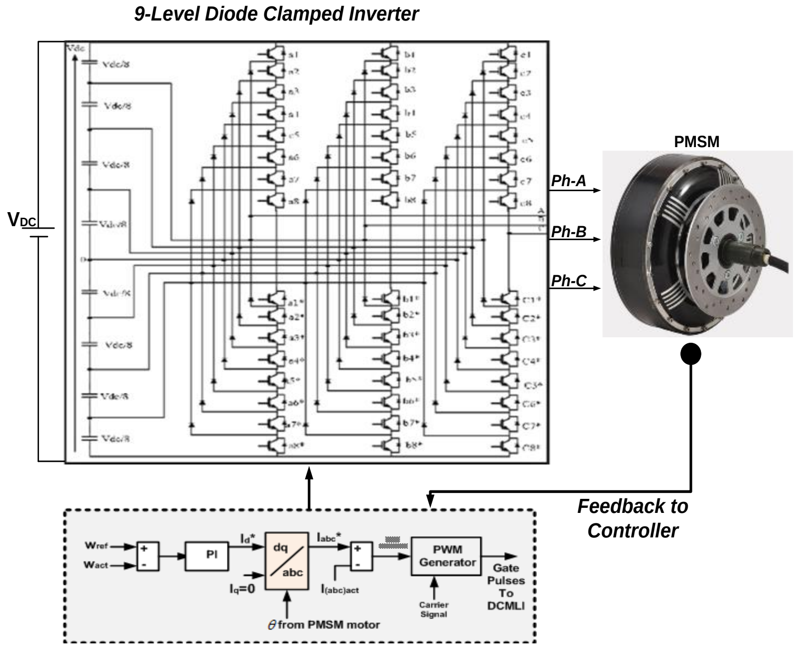


Figure 6: 9-level DCMLI fed PMSM with control

## VI. ANFIS CONTROLLER

In this section basics of ANFIS and development of ANFIS controller are given. ANFIS uses the neural network's ability to classify data and find patterns. It then develops a fuzzy expert system that is more transparent to the user and also less likely to produce memorization error than a neural network. ANFIS keeps the advantages of a fuzzy expert system, while removing (or at least reducing) the need for an expert.

The problem with ANFIS design is that large amounts of training data require developing an accurate system. The ANFIS, first introduced by Jang in 1993, is a universal approximator and, as such, is capable of approximating any real continuous function on a compact set to any degree of accuracy. ANFIS is a method for tuning an existing rule base with a learning algorithm based on a collection of training data.

This allows the rule base to adapt. As a simple example, a fuzzy inference system with two inputs x and y and one output z is assumed. The first-order Sugeno fuzzy model, a typical rule set with two fuzzy If–Then rules can be expressed as

Rule 1: If x is A1 and y is B1, then f1=p1x+q1y+r1

Rule 2: If x is A2 and y is B2, then f2=p2x+q2y+r2

The resulting Sugeno fuzzy reasoning system is shown here, the output *z* is the weighted average of the individual rules outputs and is itself a crisp value. The corresponding ANFIS architecture is shown in.

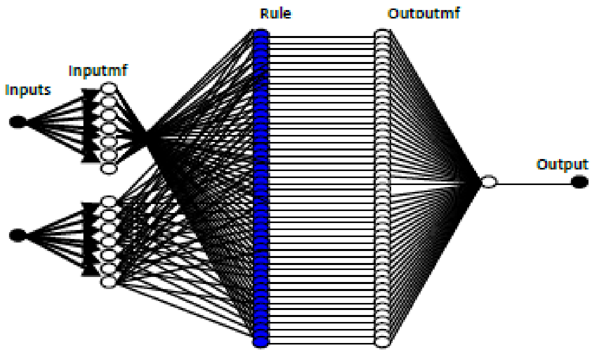


Fig: ANFIS architecture

## VII. RESULTS AND ANALYSIS

### *A. PMSM with fixed speed*

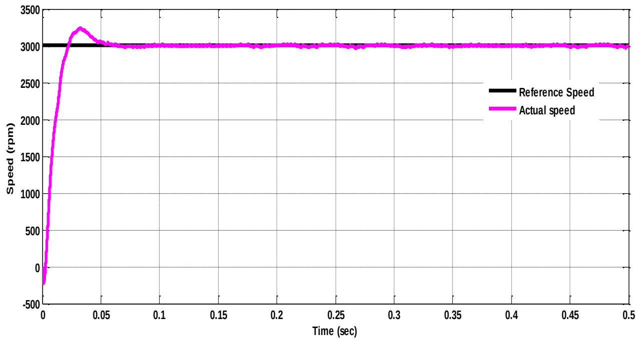


Figure 7: Speed of PMSM drive

Speed of PMSM running with fixed speed condition is shown in figure 7. Reference speed signal and the actual speed (in blue) signal are shown in figure 7. The actual speed follows the reference speed 3000 RPM. Actual speed rises to final value and PMSM runs at constant 3000 RPM.

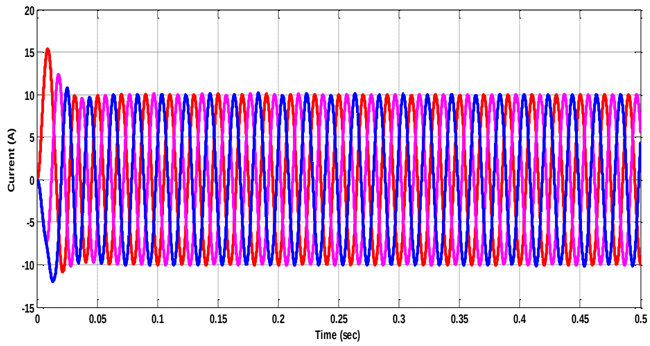


Figure 9: Three-Phase stator currents of PMSM

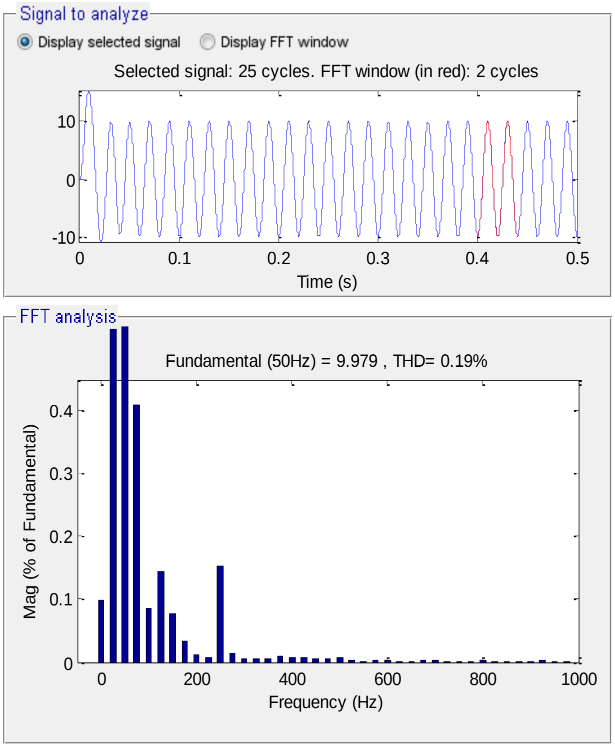


Figure 10: THD in stator current

Figure 9 illustrates three-phase stator currents of PMSM. Three-phase PMSM stator coils draws 10A current. Magnitude in three phases of stator coils remains with constant peak. Harmonic distortion FFT window of stator current is shown in figure 10. Stator current is distorted by 0.19% and is well within nominal distortion limits.

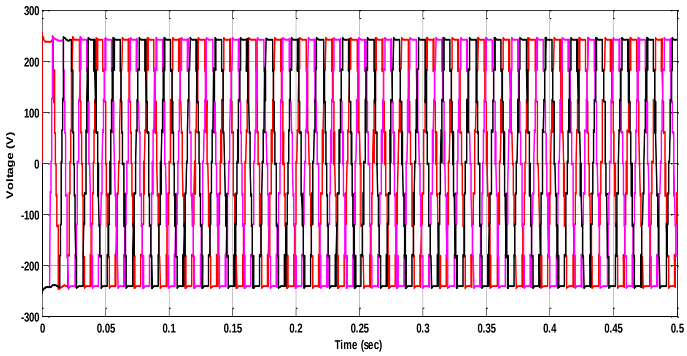


Figure 11: Three-Phase voltages of DCMLI

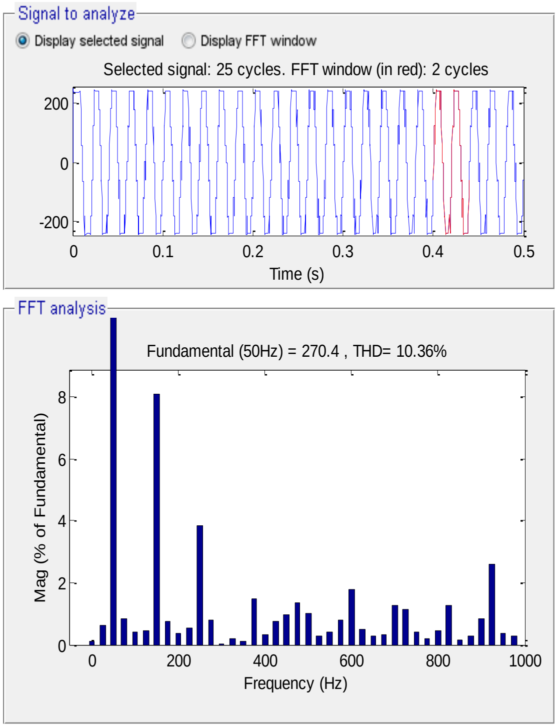


Figure 12: THD in phase voltage of DCMLI

Figure 11 illustrates three phase voltages of diode clamped inverter. Phase voltage is leveled with nine magnitudes yielding nine-level voltage signal. Peak magnitude of phase voltage in three phases is 250V. Harmonic analysis in phase voltage signal is shown in figure 12. FFT window displayed shows 10.36% distortion in phase voltage of DCMLI.

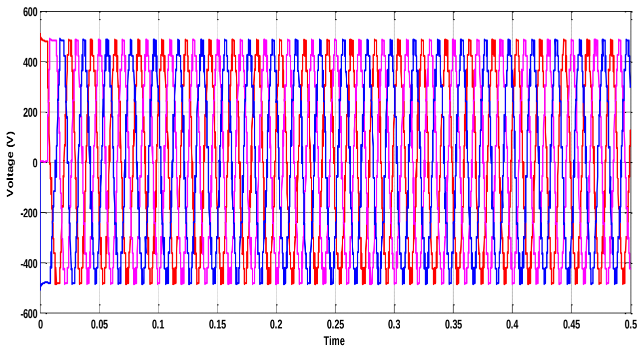


Figure 13: Three-Phase Line voltages of DCMLI

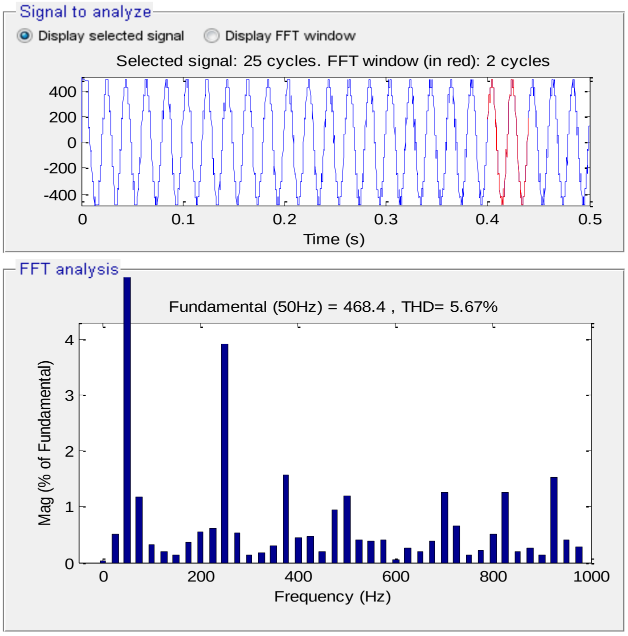


Figure 14: THD in line voltage of DCMLI

Figure 13 illustrates three-phase line voltages of diode clamped inverter. Peak magnitude of line voltage in three phases is 500V.. Harmonic analysis in line voltage signal is shown in figure 14. FFT window displayed shows 5.67% distortion in line voltage of DCMLI.

### *B. PMSM with variable speed*

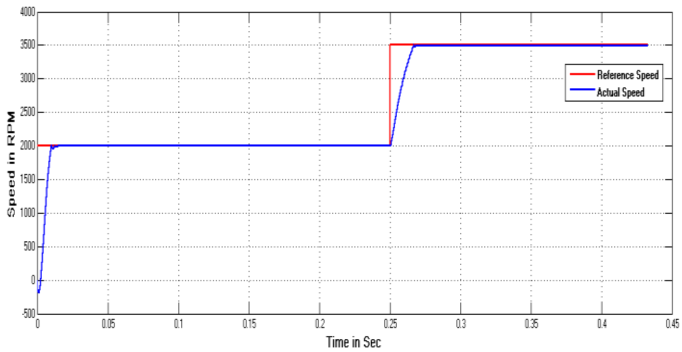


Figure 15: Speed of PMSM drive

Speed of PMSM running with variable speed condition is shown in figure 15. Reference speed signal (green) and the actual speed (blue) signal are shown in figure 15. The actual speed follows the reference speed as shown in figure. Initial PMSM run speed reference value is set to 2000 RPM and PMSM follows the set speed and continues to run at 2000 RPM. At time 0.25 seconds, reference speed command is set to 3500 RPM. The closed-loop speed control sets PMSM to follow the reference speed command and hence after 0.25 seconds PMSM speed rises to 3500 RPM and follows reference speed.

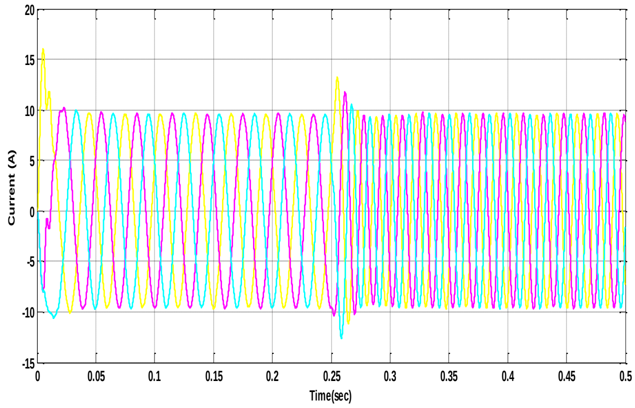


Figure 17: Three-Phase stator currents of PMSM

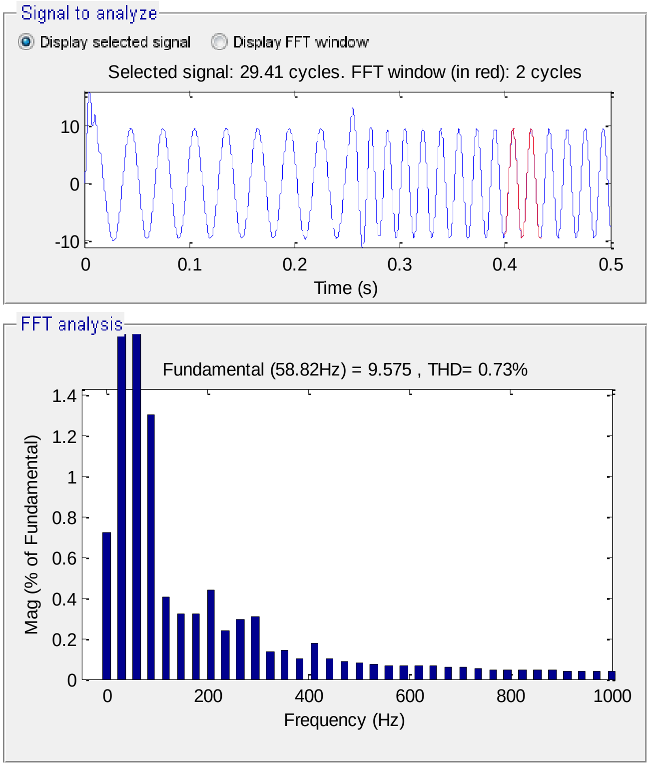


Figure 18: THD in stator current

Figure 17 illustrates three-phase stator currents of PMSM. Three-phase PMSM stator coils draws 10A current. Magnitude in three phases of stator coils remains with constant peak. As speed change command is given at 0.25 seconds, the frequency of the stator currents increases with the same 10A peak. As the speed in synchronous machines varies with frequency with constant number of stator poles, PMSM stator current frequency increases after speed is increased from 2000RPM to 3500RPM at 0.25 seconds. Harmonic distortion FFT window of stator current is shown in figure 18. Stator current is distorted by 0.73% and is well within nominal distortion limit.

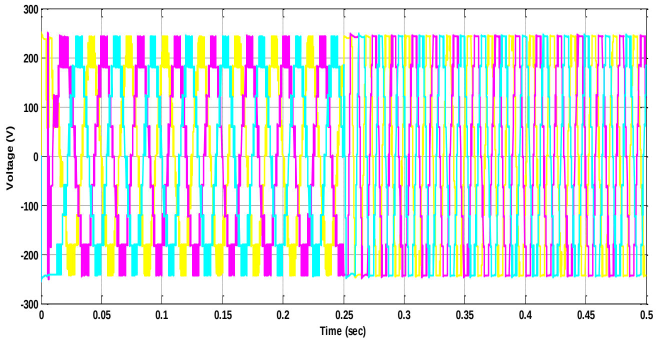


Figure 19: Three-Phase voltages of DCMLI

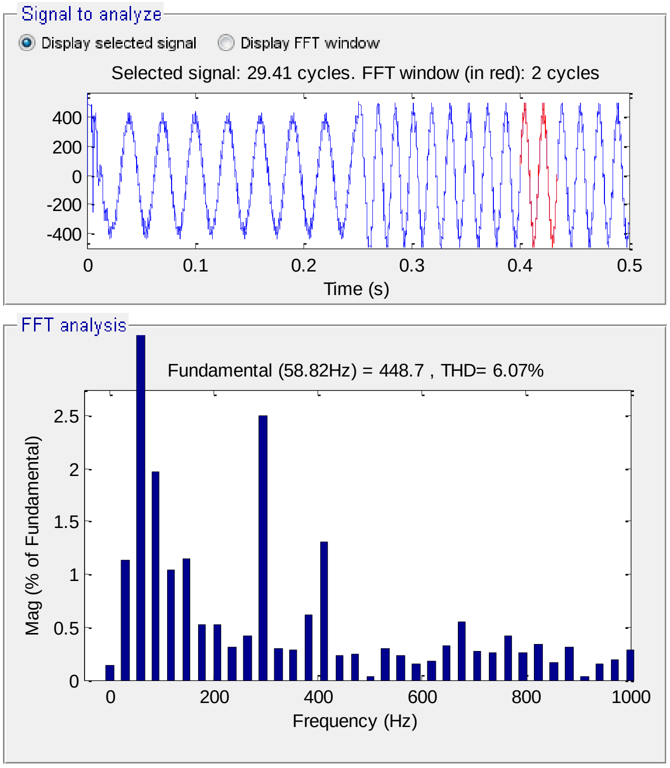


Figure 20: THD in phase voltage of DCMLI

Figure 19 illustrates three phase voltages of diode clamped inverter. Phase voltage is leveled with nine magnitudes yielding nine-level voltage signal. Peak magnitude of phase voltage in three phases is 250V. As speed change command is given at 0.25 seconds, the frequency of the phase voltages in DCMLI increases with the same peak magnitude. As the speed in synchronous machines varies with frequency with constant number of stator poles, PMSM phase voltage frequency increases proportionally after speed is increased from 2000RPM to 3500RPM at 0.25 seconds. Harmonic analysis in phase voltage signal is shown in figure 20. FFT window displayed shows 6.07% distortion in phase voltage of DCMLI.

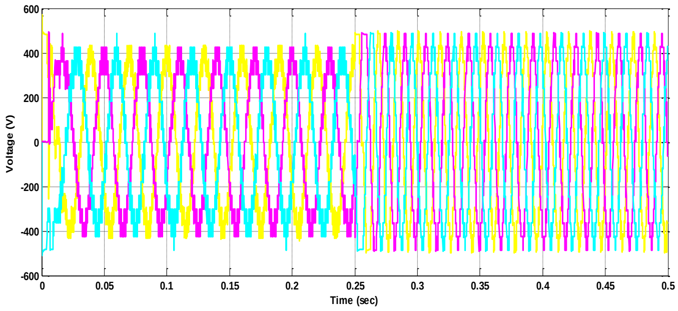


Figure 21: Three-Phase Line voltages of DCMLI

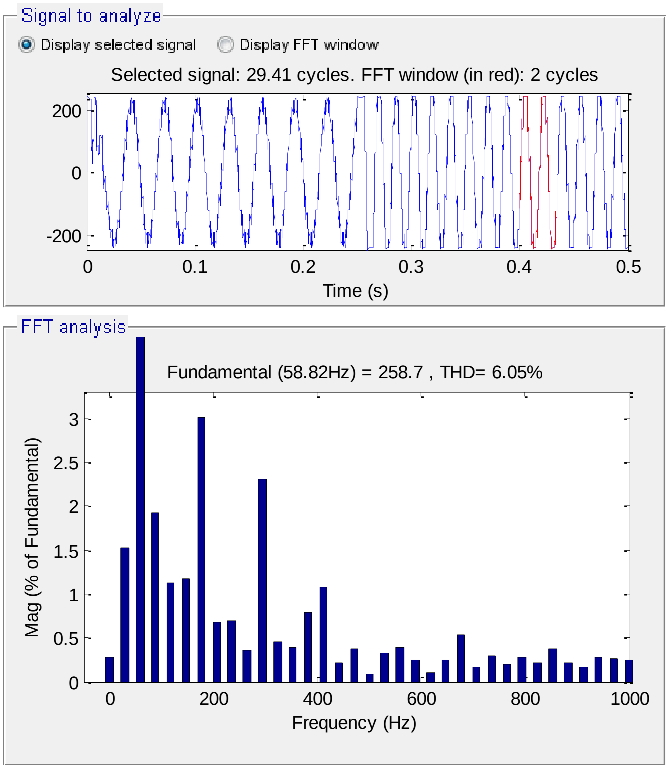


Figure 22: THD in line voltage of DCMLI

Figure 21 illustrates three-phase line voltages of diode clamped inverter. Peak magnitude of line voltage in three phases is 500V. Phase-A is illustrated in red colour, phase-B in green and phase-C in blue colour. As speed change command is given at 0.25 seconds, the frequency of the line voltage of DCMLI increases with the same peak magnitude. As the speed in synchronous machines varies with frequency with constant number of stator poles, PMSM line voltage frequency proportionally increases after speed is increased from 2000RPM to 3500RPM at 0.25 seconds. Harmonic analysis in line voltage signal is shown in figure 22. FFT window displayed shows 6.05% distortion in line voltage of DCMLI. Table III illustrates the comparison of harmonic distortion analysis in different modes of PMSM operation with different levels [12,13] of DCMLI.

THD for Fixed speed PMSM Drive

| Parameter | THD% |
|---|---|
| Stator current | 0.19% |

| | |
|---|---|
| Line Voltage | 7.90% |
| Phase Voltage | 13.53% |

THD for Variable speed PMSM Drive

| Parameter | THD% |
|---|---|
| Stator current | 0.73% |
| Line Voltage | 6.07% |
| Phase Voltage | 6.05% |

## VIII. CONCLUSIONS

PMSM drives are becoming very good option for industrial and agricultural applications these days. This paper presents the analysis of nine-level diode clamped multi-level inverter fed PMSM drive with fixed and variable sped operations. Closed loop control with ANFIS controllers is analyzed with fixed and variable speed conditions. With the simple closed-loop speed control technique, actual speed follows the reference speed with both fixed speed condition and also with variable speed condition which is validated with simulation results. DCMLI operation with switching sequence is explained. Pulses to DCMLI are generated from PWM generator using LSCPWM pattern. Reference signal obtained from speed control is compared with high frequency carrier signal to generate gate pulses to DCMLI switches. The control strategy is validated for fixed speed and variable speed condition

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