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For Electric Vehicles with Hybrid Energy Sources, a Switched-Capacitor Bidirectional DC-DC Converter with a Wide Voltage Gain Range

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Abstract— ***An exchanged capacitor bidirectional DC-DC converter with a high advance up/step-down voltage gain is proposed for electric vehicles (EVs) with a half breed vitality source framework (HESS). The converter displayed has the benefits of being a basic circuit, a diminished number of parts, a wide voltage-gain extend, a low voltage stress, and a shared opinion. Likewise, the synchronous rectifiers permit zero voltage exchanging (ZVS) turn-on and turn-off without requiring any additional equipment, and the proficiency of the converter is improved. A 300W model has been created which approves the wide voltage-gain scope of this converter utilizing a variable low-voltage side (40V-100V) and to give a consistent high-voltage side (300V). The greatest effectiveness of the converter is 94.45% in step-down mode and 94.39% in step-up mode. The test results additionally approve the possibility and the adequacy of the proposed topology.***

Index Terms—Switched-capacitor, Synchronous rectification, Bidirectional DC-DC converter, EVs, HESS, Wide voltage-gain range

I. INTRODUCTION

To address the challenges of fossil fuels as the primary energy source for transport (including reducing stockpiles and polluting emissions) [1]-[2], electric vehicles (EVs) powered by battery systems with low or zero polluting emissions, are increasing in popularity. Although the developed advancement of batteries can provide higher population performance for EVs, the unlimited charging or discharging current (i.e. inrush current) from batteries will result in shorter battery cycle life, as well as reducing the efficiency [3]. The combination of a battery and super-capacitors as a hybrid energy source system (HESS) for electric vehicles is considered as a good way to improve overall vehicle efficiency and battery life [4]. Super-capacitors have advantages of high power density, high cycle life, and very good charge/discharge efficiency. They can also provide a large transient power virtually instantaneously and are therefore suitable for meeting sudden EV power changes such as acceleration or meeting an incline.

The HESS can make full use of the performance of batteries and super-capacitors: the super-capacitors supply power for acceleration and regenerative braking with the battery meeting the requirement of high energy storage density for long range operation [5]. A challenge for the HESS is that the terminal voltage of super-capacitors is low, and varies over a wide range as they are charged or discharged. Therefore, a bidirectional DC–DC converter with a wide voltage-gain range is desired for the HESS to connect low-voltage super-capacitors with a high-voltage DC bus. There are two broad classifications for bidirectional DC-DC converters, namely isolated converters and non-isolated converters. Isolated converters, such as half-bridge and full-bridge topologies are implemented using a transformer [6]-[8]. In addition, the half-bridge converter in [6] needs a center-tapped transformer which results in a complex structure, and the full-bridge converters in [7]-[8] require a higher number of semiconductor devices. High-frequency transformers and coupled inductors can be used in isolated converters to obtain high step-up and step-down ratios [9]-[11]. However, in [9], the realization of bidirectional power flow requires ten power semiconductors and two inductors. The converter in [10] requires two inductors in addition to the transformer, and three inductors are used for the converter in [11]. The structure of these converters is complex, the cost is high, and it is difficult to standardize the design. When the turns ratio of the high frequency transformer increases, the number of winding turns increase correspondingly and the leakage inductance of the transformer may result in high voltage spikes across the main semiconductors during switching transitions. In order to reduce the voltage stress caused by the leakage inductance, a bidirectional DC-DC converter with an active clamp circuit in [12] and a full bridge bidirectional DC-DC converter with a Fly back snubber circuit in [13] were proposed. Besides, the dual active bridge converter in [14] and the phase-shift full-bridge converter in [15] also utilized the leakage inductance to achieve the soft-switching, and the energies stored in the leakage inductance were transferred to the load. When the input and output voltages do not match

the turns ratio of the transformer, the power switch losses will increase dramatically [16], which reduces the efficiency of the converter. For non-isolated topologies, such as Cuk and Sepic/zeta converters, their efficiencies are low [17], [18] as they use cascaded configurations of two power stages. Conventional buck-boost converters are good candidates for low-voltage applications due to their high efficiency and low cost. Unfortunately, the drawbacks of narrow voltage conversion range, high voltage stress and extreme duty cycle for the semiconductors make them unsuitable for application to EV HESS. The voltage gain of the bidirectional DC-DC converter in [19] is greatly improved, but the voltage stress across the power semiconductors is still equal to that of the high voltage side. The voltage stress across the power semiconductors of the bidirectional three-level DC-DC converters in [20] and [21] is half that of conventional buck-boost converters, but its voltage-gain range is still small. In addition, the low-voltage and high-voltage side grounds of this converter are connected by a power semiconductor, and therefore the potential difference between the two grounds is a high frequency PWM voltage, which may result in extra maintenance issues and EMI problems. The low-voltage and high-voltage sides of the bidirectional three-level DC-DC converter in [22] share a common ground, but the voltage-gain of this converter is still limited. In addition, this converter requires complicated control scheme to balance the flying-capacitor voltage. A high bidirectional voltage conversion ratio with lower voltage stresses across the power semiconductors can be achieved by the converter of [23] with a reasonable duty ratio, but the converter still has many problems such as a large number of components, and a high frequency PWM voltage between the low-voltage and high-voltage sides. The multi-level converter in [24] can achieve a high voltage gain with low voltage stress across the power semiconductors. However, this converter needs a higher number of power semiconductors which leads to increased losses and higher cost. Switched-capacitor converter structures and control strategies are simple and easy to expand.

They use different charging and discharging paths for the capacitors to transfer energy to either the low-voltage or the high-voltage side to achieve a high voltage gain. Thus, the switched-capacitor converter is considered to be an effective solution to interface the super-capacitors with the high voltage DC bus. Single capacitor bidirectional switched-capacitor converters were proposed in [25], [26], but the converter's efficiency is low. The efficiency of the converter in [27] has been improved through soft-switching technology, but it required many extra components. [28] proposed a multi-level bidirectional converter with very low voltage stress across the power semiconductors, but twelve semiconductors are needed, and the drawbacks of low voltage gain, complex control and structure limit its application. The high voltage gain bidirectional DC-DC converters in [29], [30] need only four semiconductors. However, the maximum voltage stress of the converter in [29] is that of the high voltage side, and the maximum voltage stress of the converter in [30] is higher than that of the high voltage side, which will increase switching losses and reduce the conversion efficiency of these converters. The bidirectional converter in [31] only requires three semiconductors, but its voltage-gain range is still small. In addition, the low-voltage and high-voltage side grounds of this converter are connected by an inductor, which will also generate extra EMI problems. Finally, the converter in [32] has improved the conversion efficiency greatly, but it needs three inductors and a higher number of power semiconductors which increases the conduction losses and makes the design more challenging. Although exponential switched-capacitor converters have high step-up capabilities, they operate relatively poorly with respect to the switch and capacitor voltage stresses, as they involve several different higher voltage levels [33]. To meet the requirements for the bidirectional converter for the super-capacitor in an EV HESS, a high ratio bidirectional DC-DC converter which uses synchronous rectification is proposed in this paper, as show in Fig. 1. The main contribution of the proposed converter lies in the integrated advantage of having a wide voltage-gain range, in the case of requiring less number of components with the reduced voltage stress. In addition, the synchronous rectifiers allow ZVS turn-on and turn-off without requiring any extra hardware. The efficiency of the power conversion is therefore improved, as well as the utilization of the power switches. Although the proposed converter has a high voltage gain, it is built without the magnetic coupling, and it can simplify the converter design due to eliminating the need for coupled-inductor. Finally, the proposed converter is suitable for EV applications because its input inductor can provide a continuous current, and the switched-capacitors can also be taken advantage of efficiently with the dynamic balanced switched-capacitor voltages. The paper is organized as follows. In Section II, the topology of the switched-capacitor bidirectional DC-DC converter is presented. In Section III, the operating principles of the proposed converter are analyzed. The steady-state characteristics of the converter are analyzed in Section IV and experimental results are presented in Section V.

II. THE PROPOSED CONVERTER

Fig. 1 shows the proposed switched-capacitor bidirectional DC-DC converter which is composed of four power semiconductors Q1-Q4, four capacitors and one inductor L. Clow, and Chigh are the energy storage/filter capacitors of the low-voltage and high-voltage sides, and C1, C2 are the switched capacitors. L is an energy storage/filter inductor. In addition, power semiconductors Q2-Q4, and C1, C2, Chigh form the switched-capacitor network, including switched-capacitor units C1-Q2, C2-Q3 and Chigh-Q4. ilow, ihigh are the currents through the low-voltage and high-voltage sides, Ulow, UC1, UC2, Uhigh are the voltages across Clow, C1, C2 and Chigh, respectively.

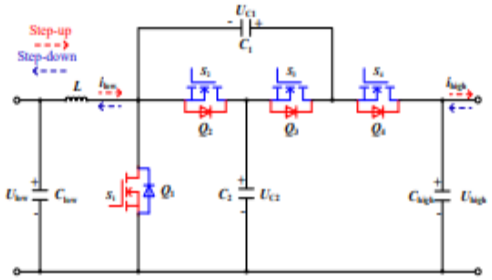


Fig. 1 The proposed topology of the switched-capacitor bidirectional DC-DC converter.

III. OPERATING PRINCIPLES

To simplify the steady-state analysis of the proposed converter, the operating conditions are assumed to be as follows:

(a) all the power semiconductors and energy storage components of the converter are treated as ideal, and the converter operates in the continuous conduction mode (CCM).

(b) all the capacitances are large enough that each capacitor voltage is considered constant over each switching period.

A. Step-Up Mode When the energy flows from the low-voltage side to the high-voltage side, the output voltage Uhigh is stepped up from Ulow by controlling the power semiconductor Q1, and the anti-parallel diodes of Q2, Q3 and Q4. UQ1, UQ2, UQ3 and UQ4 are the voltage stresses across the corresponding power switches in step-up mode. d1=dBoost is the duty cycle of Q1. Fig. 2 shows the typical waveforms in the step-up mode, and Fig. 3 shows the current-flow paths of the proposed converter.

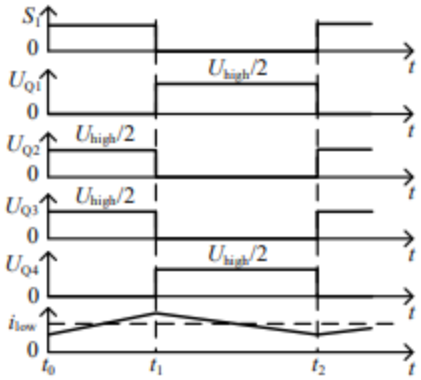
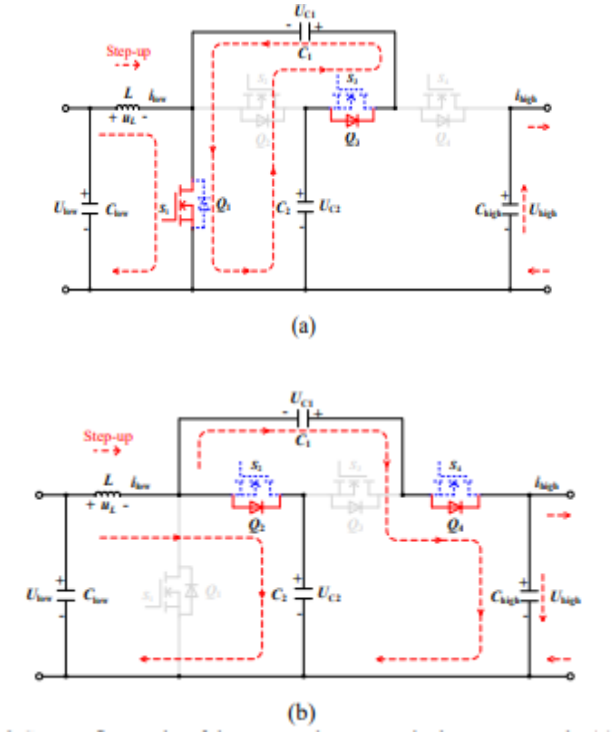


Fig. 2 Typical waveforms of the proposed converter in step-up mode.



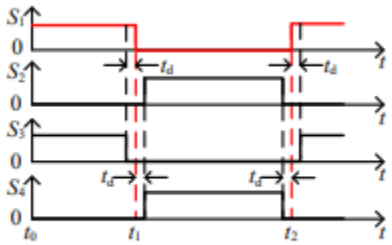
(a)

(b)

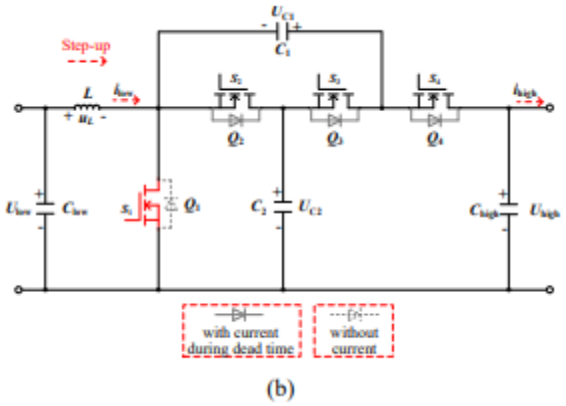
Fig. 3 Current-flow paths of the proposed converter in the step-up mode. (a) Mode I S1=1. (b) Mode II S1=0.

Mode I: Power semiconductor Q1 is turned on. The anti-parallel diode of Q3 turns on, while the anti-parallel diodes of Q2 and Q4 turn off. The current-flow paths of the proposed converter are shown in Fig. 2(a). The energy of the DC source Ulow is transferred to inductor L. Meanwhile, C1 is being charged by capacitor C2. Chigh provides energy for the load.

Mode II: Power semiconductor Q1 and the anti-parallel diode of Q3 are off, while the anti-parallel diodes of Q2 and Q4 are on. The current-flow paths of the proposed converter are shown in Fig. 2(b). C2 charges from inductor L. Meanwhile, C1 is discharging and Chigh is charging. The DC source Ulow, L and C1 provide energy for the load. As shown in Fig. 2 and Fig. 3, when the proposed switched-capacitor bidirectional converter operates in the step-up mode, the currents flow into the corresponding anti-parallel diodes. This will result in lower efficiency, as well as lower utilization of the power semiconductors. Therefore, a high step-up/step-down ratio switched-capacitor bidirectional DC-DC converter with synchronous rectification is proposed further in this paper.



(a)



(b)

Fig. 4 Synchronous rectification operating principle for the proposed bidirectional converter. (a) Gate signals and dead time in the step-up mode. (b) Current-flow paths in the step-up mode.

Fig. 4 shows the principle of operation of the synchronous rectification for the proposed switched-capacitor bidirectional DC-DC converter in the step-up mode. The power semiconductor Q1 switches according to the gate signal S1 shown in Fig. 4(a). During the dead time td, the current must flow in the corresponding anti-parallel diodes of Q2, Q3 and Q4, as shown in Fig. 4(b). Otherwise, the current will flow in the controlled power semiconductors Q2, Q3 and Q4 due to their lower on-state resistance and on-state voltage drop using the gate signals S2, S3 and S4 shown in Fig. 4(a). In addition, when Q2, Q3 and Q4 are operating in synchronous rectification, their gate signals will be turn-off in advance by the dead-time td. During the dead-time td, the currents flow in the corresponding anti-parallel diodes of Q2, Q3 and Q4, and their voltage stress across them are close to zero due to the forward voltage drops of the anti-parallel diodes, as shown in Fig. 4(b). As a result, the controlled MOSFETs of Q2, Q3 and Q4 are turned off with the ZVS. Similarly, the gate signals of Q2, Q3 and Q4 will be turn-on by delaying the dead-time td. The currents flow in the corresponding anti-parallel diodes of Q2, Q3 and Q4 during the dead-time td, and then flow in the controlled MOSFETs of Q2, Q3 and Q4 due to their lower on-state resistance, as shown in Fig. 4(b). As a result, the controlled MOSFETs of Q2, Q3 and Q4 are also turned on with the ZVS. Thus, the efficiency of the converter can be further improved.

B. Step-Down Mode When energy flows from the high-voltage side to the low-voltage side, the output voltage Ulow is stepped down from Uhigh by controlling the power semiconductors Q2, Q3 and Q4, and the anti-parallel diode of Q1. UQ1, UQ2, UQ3 and UQ4 are the voltage stresses across the corresponding power switches in step-down mode. The relationship between d2 and d4 can be written as d2=d4=dBuck, where d2 and d4 are the duty cycles of Q2 and Q4 respectively. Fig. 5 shows the typical waveforms in the step-down mode, and Fig. 6 shows the current-flow paths of the proposed converter.

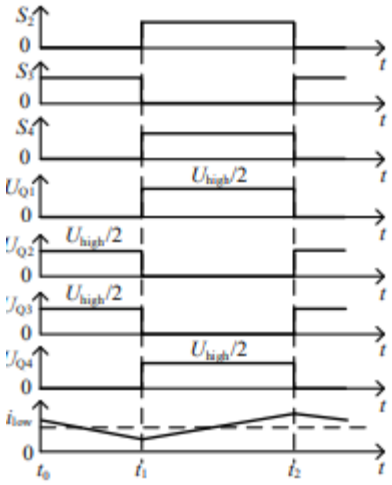
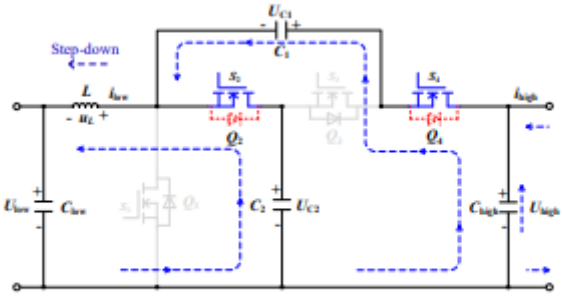


Fig. 5 Typical waveforms of the proposed converter in step-down mode.

Mode I: Power semiconductors Q2 and Q4 are turned on. Power semiconductor Q3 and the anti-parallel diode of Q1 are off. The current-flow paths of the proposed converter are shown in Fig. 6(a). L is charging from capacitor C2. Meanwhile, C1 is charging from Chigh and Uhigh. The DC source Uhigh, L and C2 provide energy for the load.

Mode II: Power semiconductor Q3 and the anti-parallel diode of Q1 turn on, while power semiconductors Q2 and Q4 turn off. The current-flow paths of the proposed converter are shown in Fig. 6(b). L is discharging. Meanwhile, C2 is charging from capacitor C1, and Chigh is charging from Uhigh. L provides energy for the load. Fig. 7 shows the synchronous rectification operating principle for the proposed switched-capacitor bidirectional DC-DC converter in the step-down mode. The power semiconductors Q2, Q3 and Q4 switch according to gate signals S2, S3 and S4 shown in Fig. 7(a). During the dead time td, the current must flow in the corresponding anti-parallel diodes of Q1, as shown in Fig. 7(b). Otherwise, the current can flow in the controlled power semiconductors Q1 due to its lower on-state resistance and on-state voltage drop using the gate signal S1 shown in Fig. 7(a). As a result, the controlled MOSFET of the synchronous rectifier Q1 is also turned on and turned off with ZVS.



(a)

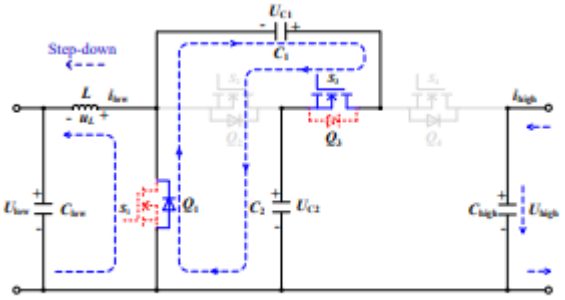
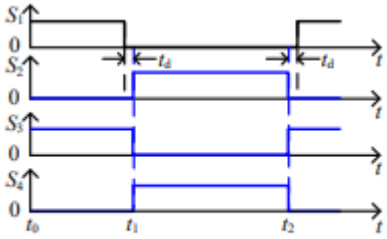


Fig. 6 Current-flow paths of the proposed converter in the step-down mode. (a) Mode I S2S3S4=101. (b) Mode II S2S3S4=010.



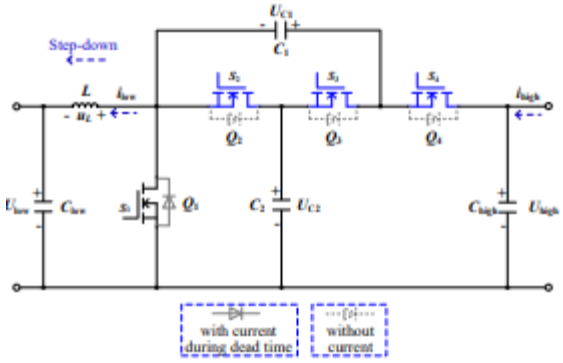


Fig. 7 Synchronous rectification operation principle of the proposed bidirectional converter. (a) Gate signals and dead time in the step-down mode. (b) Current-flow paths in the step-down mode.

C. Control strategy of bidirectional power flow

Based on the operating principles previously described, the bidirectional power flow control strategy can be illustrated as shown in Fig. 8. The block diagram representation of the experimental configuration is shown in Fig. 8(a). The voltages Uhigh and Ulow, and the current ilow are obtained by sampling the sensors, and the converter voltage and current loops are implemented on a TMS320F28335 DSP controller.

As shown in Fig. 8(b), the proposed bidirectional DC-DC converter switches between the step-up and the step-down modes, according to the power flow control signal Uc which is calculated by the TMS320F28335 DSP controller. It operates in the step-up mode when Uc=0, the voltage Uhigh is controlled by the voltage controller

with the reference voltage Uref-Boost in the voltage-loop. Meanwhile, the feedback current i_{low} is controlled by the current controller using the reference current Iref-Boost in the current-loop. The corresponding PWM schemes as shown in Fig. 2 and Fig. 4(a) are selected to generate the gate signals S1~S4 in the step-up mode. In a similarly way, the converter operates in the step-down mode when Uc=1: the voltage Ulow is controlled by the voltage controller with the reference voltage Uref-Buck, and the feedback current ilow is controlled by the current controller with the reference current Iref-Buck, (which has the opposite polarity to the reference current Iref-Boost). The corresponding PWM schemes as shown in Fig. 5 and Fig. 7(b) are also selected to generate the gate signals S1~S4 in the step-down mode.

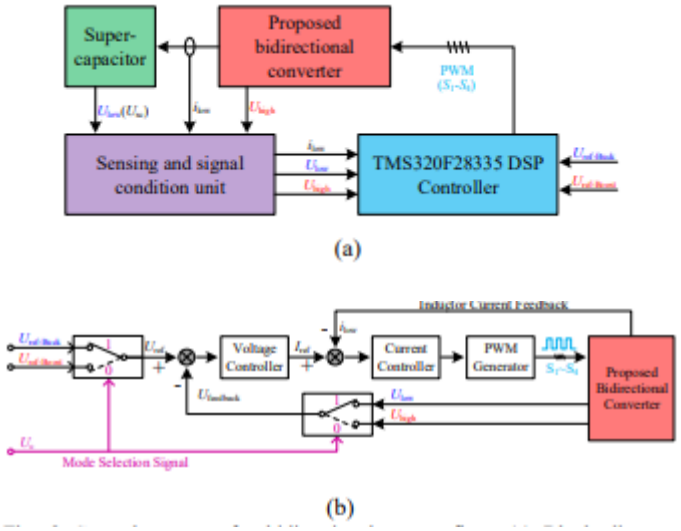


Fig. 8 Control strategy for bidirectional power flow. (a) Block diagram representation of experimental configuration. (b) Realization of double closed-loop control strategy.

IV. ANALYSIS OF STEADY-STATE CHARACTERISTICS

A. Voltage-gain in steady-state (1)

Voltage-gain in step-up mode As shown in Fig. 2 and Fig. 3(a), C1 and C2 are connected in parallel when S1=1, so that the voltages across C1 and C2 are equal. According to Fig. 3(a, b) and the volt-second balance principle on L, the following equations can be obtained:

$$\begin{cases} d_{\text{Boost}} \times U_{\text{low}} = (1-d_{\text{Boost}}) \times (U_{C2} - U_{\text{low}}) \\ U_{C1} + U_{C2} = U_{\text{high}} \\ U_{C1} = U_{C2} \end{cases} \quad (1)$$

Therefore, by simplifying (1), the following equation can be written:

$$\begin{cases} U_{C1} = U_{C2} = \dfrac{1}{1-d_{\text{Boost}}} U_{\text{low}} \\ U_{\text{high}} = \dfrac{2}{1-d_{\text{Boost}}} U_{\text{low}} \end{cases} \quad (2)$$

Based on the law of energy conservation,

$I_{\text{low}} \times U_{\text{low}} = U_{\text{high}} \times I_{\text{high}}$. Therefore:

$$I_{\text{low}} = \frac{2}{1-d_{\text{Boost}}} I_{\text{high}} \quad (3)$$

where I_{low} and Ihigh are the average currents of i_{low} and i_{high} respectively in the step-up mode. According to (2), the voltage-gain of the proposed converter in the step-up mode is 2/(1-dBoost), which is twice as large as the voltage-gain of the conventional buck-boost converter. In addition, the voltage stress of C1 and C2 can be reduced to half of the output voltage U_{high}.

(2) Voltage-gain in the step-down mode As shown in Fig. 5 and Fig. 6(b), C1 and C2 are connected in parallel when S2S3S4=010, so that the voltages of C1 and C2 are equal. According to Fig. 6(a, b) and the volt-second balance principle on L, the following equation can be obtained:

$$\begin{cases} d_{\text{Buck}} \times (U_{C2} - U_{\text{low}}) = (1 - d_{\text{Buck}}) \times U_{\text{low}} \\ U_{C1} + U_{C2} = U_{\text{high}} \\ U_{C1} = U_{C2} \end{cases} \quad (4)$$

Therefore, by simplifying (4), the following equation can be written:

$$\begin{cases} U_{C1} = U_{C2} = \dfrac{1}{2} U_{\text{high}} \\ U_{\text{low}} = \dfrac{d_{\text{Buck}}}{2} U_{\text{high}} \end{cases} \quad (5)$$

By substituting $I_{\text{low}} \times U_{\text{low}} = U_{\text{high}} \times I_{\text{high}}$ in (5):

$$I_{\text{high}} = \frac{d_{\text{Buck}}}{2} I_{\text{low}} \quad (6)$$

where I_{low} and I_{high} are the average currents of i_{low} and i_{high} respectively in the step-down mode. According to (5), the voltage-gain of the proposed converter in the step-down mode is dBuck/2, which is half of the voltage-gain of the conventional buck-boost converter. In addition, the voltage stress of C1 and C2 are still half of the input voltage U_{high}.

B. Voltage and current stresses of power semiconductors

(1) Voltage stress As shown in Fig. 3(a) in the step-up mode and Fig. 6(b) in the step-down mode, Q1 is turned on and Q2 is turned off, so that Q2 and C2 are connected in parallel. Therefore the voltages across Q2 and C2 are equal. Similarly, the voltages across the other power semiconductors can also be obtained. According to (2) in the step-up mode and (5) in the step-down mode, the voltage stress for the power semiconductors can be written as:

$$\begin{cases} U_{Q1} = U_{C2} = \dfrac{U_{\text{high}}}{2} \\ U_{Q2} = U_{Q3} = U_{C1} = \dfrac{U_{\text{high}}}{2} \\ U_{Q4} = U_{\text{high}} - U_{C2} = \dfrac{U_{\text{high}}}{2} \end{cases} \quad (7)$$

Based on (7), all the voltage stresses of the power semiconductors and switched capacitors C1 and C2 are half of

(2) Current stress

According to Fig. 3 and (3), the current stress of the power semiconductors in the step-up mode can be obtained by applying the ampere-second balance principle on C1, C2 and Chigh as follows.

$$\begin{cases} I_{Q1} = \left(\dfrac{2}{1 - d_{\text{Boost}}} + \dfrac{1}{d_{\text{Boost}}}\right) I_{\text{high}} \\ I_{Q2} = I_{Q4} = \dfrac{1}{1 - d_{\text{Boost}}} I_{\text{high}} \\ I_{Q3} = \dfrac{1}{d_{\text{Boost}}} I_{\text{high}} \end{cases} \quad (8)$$

In a similar way, according to Fig. 6 and (6), the current stress of the power semiconductors in the step-down mode can be obtained as (9)

$$\begin{cases} I_{Q1} = \left[1 + \dfrac{d_{Buck}}{2(1-d_{Buck})}\right] I_{low} \\ I_{Q2} = I_{Q4} = \dfrac{1}{2} I_{low} \\ I_{Q3} = \dfrac{d_{Buck}}{2(1-d_{Buck})} I_{low} \end{cases} \quad (9)$$

Based on (8) and (9), it can be seen that the current stress of Q1 is slightly higher than that of the power semiconductors of a conventional buck-boost converter operating under the same conditions. However it is easier (and cheaper) to choose a MOSFET with a higher rated current than the one with a higher rated voltage. Furthermore, the proposed switched-capacitor bidirectional converter can obtain a high voltage gain while the duty cycle is in the range 0.5<dBoost<dBuck high side voltage U_{high}, rather than Uhigh/2. For the converter proposed in this paper, the number of main components is between those of the converters described in [22] and [30] , the voltage stress across all the semiconductors is $U_{high}/2$, and its voltage gain is higher than that of [22] . When the step-up voltage gain is 6.25, the efficiency of the converter in [30] is approximately equal to 91.2%, while the proposed converter's conversion efficiency is 91.9% with the same voltage gain. Moreover, the efficiency of the converter in [22] is nearly equal to 90% when U_{low}=220V, U_{high}=340V, and Pn=300W, while the proposed converter's efficiency reaches 94.39% when Ulow=100V, U_{high}=300V, and Pn=300W.

TABLE I Comparisons between proposed and other bidirectional solutions.

Bidirectional Solution	Voltage Gain	Number of Switches	Number of Inductors	Voltage Stress
Buck/Boost converter	$\frac{1}{1-d}$	2	1	U_{high}
Converter in [22]	$\frac{1}{1-d}$	4	1	$U_{high}/2$
Converter in [29]	$\frac{2}{1-d}$	4	2	$U_{high}/2$, U_{high}
Converter in [30]	$\frac{1}{(1-d)^2}$	4	2	$U_{high}(1\text{-}d)$, U_{high}, $U_{high}+U_{high}(1\text{-}d)$
Proposed Converter	$\frac{2}{1-d}$	4	1	$U_{high}/2$

V. EXPERIMENTAL RESULTS AND AYALYSIS

In order to validate the theoretical analysis, a 300W experimental prototype for the proposed switched-capacitor bidirectional DC-DC converter was developed, as shown in Fig. 9. The parameters of the experiment rig are shown in Table II.

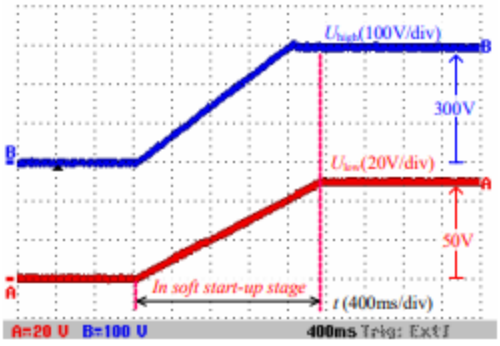
TABLE II Experiment parameters.

Parameters	Values
Rated power P_n	300W
Storage/filter capacitors C_{low} and C_{high}	520 μF
Switched-capacitors C_1 and C_2	520 μF
Storage/filter inductor L	353 μH
High side voltage U_{high}	300 V
Low side voltage U_{low}	40~100 V
Switching frequency f_s	20 kHz
Power semiconductors Q_1~Q_4	IXTK 88N30P

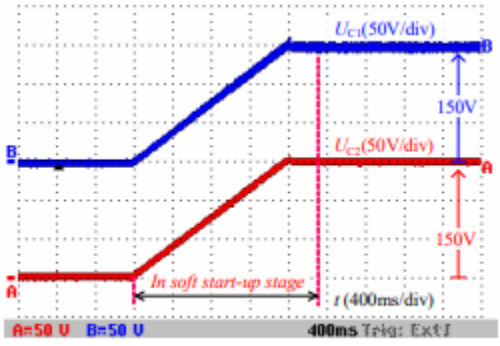
Fig. 9 The experimental prototype of the proposed switched-capacitor bidirectional DC-DC converter.

A. Experimental results in the step-up mode

In order to build the initial voltages across the switched capacitors and eliminate the inrush current when the converter starts up, a soft-starting circuit is adopted between the battery and the input side of the proposed converter in this paper. Then, the low voltage battery and the high voltage DC bus are interfaced by the proposed bidirectional DC-DC converter, and the experimental results are shown in Fig. 10. In Fig. 10(a), when the converter starts up, the input voltage Ulow rises from 0 to 50V gradually over 2 seconds, due to the soft-starting circuits. Accordingly, the output voltage rises from 0V to 300V (i.e. the reference voltage) gradually with a voltage control loop. It is noticed that the output voltage Uhigh arrives at the reference voltage (300V) before the input voltage Ulow reaches the battery voltage (50V), because the voltage control loop gets rid of the duty cycle limitation, and obtains the static state when the input voltage Ulow rises to 40V approximately. In addition, as shown in Fig. 10(b), the switched capacitor voltages UC1 and UC2 rise according to the output voltage Uhigh. It is also noticed that switched capacitor voltages UC1 and UC2 still keep at half of the output voltage Uhigh due to the voltage balance characteristic, especially in the soft start-up stage.



(a)



(b)

Fig. 10 Experimental results of the soft start-up. (a) The input voltage Ulow and the output voltage Uhigh. (b) The voltages across C1 and C2.

The voltage stress across the semiconductors and the capacitors in the step-up mode for U_{low}=40V and U_{high}=300V are shown in Fig. 11 and Fig. 12. It can be seen in Fig. 11 that the duty cycle of the active power semiconductor Q1 is dBoost=0.73, when the voltage-gain is 7.5. In addition, the PWM blocking voltage of each power semiconductor is 150V, namely half of the high-side voltage U_{high}, which validates the analysis in Section IV. The voltages across C1 and C_{high} are
shown in Fig. 12. The voltage stress of C1 is 150V, which is also half of the high-side voltage U_{high}. Therefore, the switched-capacitor bidirectional DC-DC converter can perform with a high voltage-gain and a low voltage stress across the semiconductors and the capacitors. The voltage waveforms of the synchronous rectifiers of the proposed converter in the step-up operating mode are shown in Fig. 13. The current flows through the anti-parallel diodes of Q2, Q3 and Q4 during the dead time, and the blocking voltages of Q2, Q3 and Q4 are around zero. Otherwise, the controlled MOSFETs Q2, Q3 and Q4 are turned on and turned off with ZVS by synchronous rectification. The gate signal S3 and the voltage stress of Q3 are shown in Fig. 13. In the step-up mode, the output voltage stays constant around the reference voltage 300V by the action of the voltage control loop. Fig. 14 illustrates the dynamic state of the output voltage when the input voltage is changed from 100V to 40V over a period of 10s. According to Fig. 14, when the input voltage U_{low} varies from 100V to 40V, the output voltage remains at 300V, which means the proposed converter can obtain a wide voltage-gain range varying from 3 to 7.5.

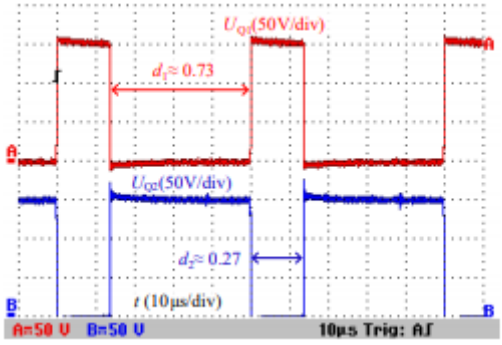


Fig. 11 The PWM voltages of power semiconductors Q1 and Q2.

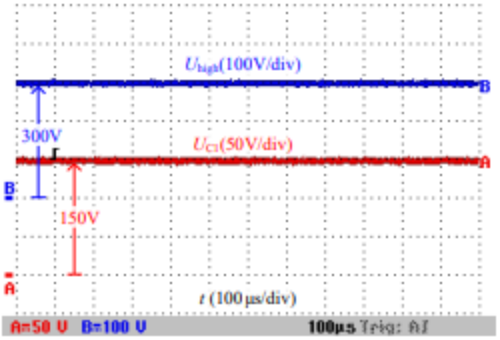


Fig. 12 Voltages across C1 and Chigh under Ulow=40V and Uhigh=300V.

B. Experimental results in the step-down

Mode The voltage stress of the semiconductors and the capacitors in the step-down mode for Ulow=40V and Uhigh=300V are shown in Fig. 15 and Fig. 16. It can be seen in Fig. 15 that the duty cycle of the active power semiconductor Q4 is dBoost=0.27, when the voltage-gain is 1/7.5. In addition, the PWM blocking voltage of each power semiconductor is 150V. The voltages across C2 and Chigh are shown in Fig. 16. The voltage stress of C2 is also 150V. Obviously, it can be concluded that the voltage stress of the semiconductors and the capacitors are also half of the high-side voltage Uhigh in the step-down mode.

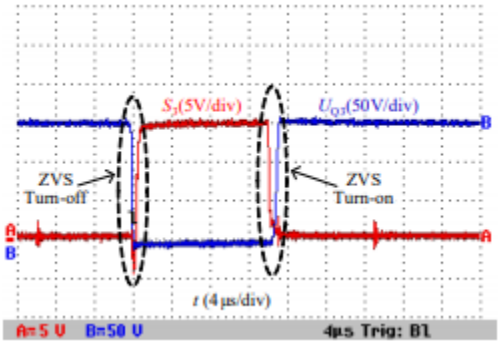


Fig. 13 Gate signal and voltage stress of synchronous rectification power semiconductor Q3.

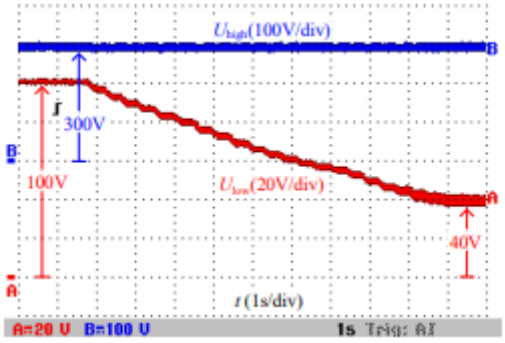


Fig. 14 The output voltage and the wide-range changed input voltage from 100V to 40V in the step-up mode.

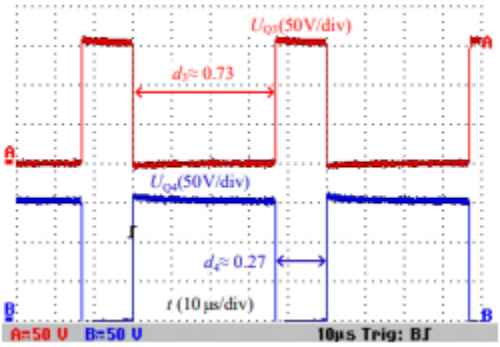


Fig. 15 The PWM voltages of power semiconductors Q3 and Q4.

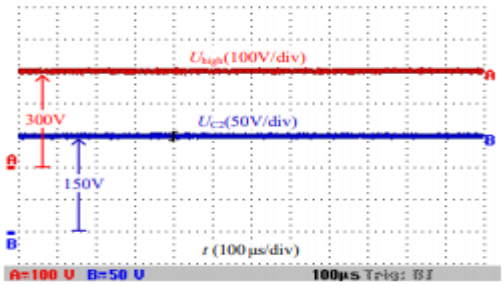


Fig. 16 Voltages across C2 and C_{high} under U_{low}=40V and U_{high}=300V.

Fig. 17 shows the voltage waveforms of the synchronous rectifier of the proposed converter in the step-down operating mode. The current flows through the anti-parallel diode of Q1 during the dead time, and the blocking voltage of Q1 is also close to zero. Otherwise, the controlled MOSFETs Q1 is turned on and turned off with ZVS by synchronous rectification, as shown in Fig. 17. Fig. 18 illustrates the dynamic state of the output voltage U_{low} and the input voltage U_{high} when the output voltage is controlled from 40V to 100V and the input voltage is kept at 300V. According to Fig. 18, under the control of the voltage loop, when the input voltage stays at 300V, the output voltage U_{low} can be controlled continuously over 8 seconds from 40V to 100V, which means the proposed converter can obtain a wide voltage-gain range varying from 1/7.5 to 1/3.

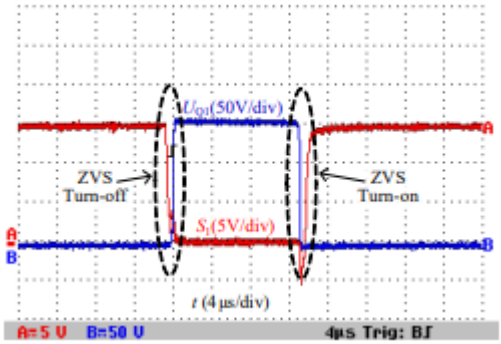


Fig. 17 Gate signal and voltage stress of synchronous rectification power semiconductor Q1.

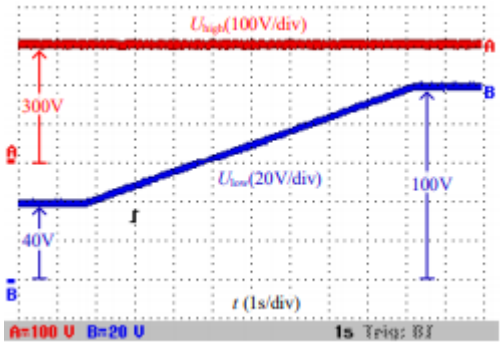


Fig. 18 The input voltage and the wide-range output voltage from 40V to 100V in the step-down mode.

C. Experiment results for bidirectional power flow control

Fig. 19 shows the EV hybrid energy source system, where the super-capacitor bank is made up of CSDWELL model MODWJ001PM031Z2 super-capacitors. The battery in the HESS is a lithium iron phosphate battery, and a resistive load Pload is used to simulate the electric vehicle load. In the HESS shown in Fig. 19, Ubat, Ibat and Pbat are the output voltage, output current and output power of the battery, Usc, Isc and Psc are the output voltage, output current and output power of the super-capacitor. In this experiment, the output voltages of the battery and the super-capacitors are 50V and 40V respectively, and the electric vehicle's power varies with step changes between 400W and 650W (the power difference 250W is provided by the super-capacitors instantaneously through the proposed converter). The proposed switched-capacitor bidirectional DC-DC converter in this paper is applied as the power interface between the super-capacitor and the DC bus, and it operates according to the control strategy shown in Fig. 8. In addition, filter control is adopted to determine the power distribution between the battery and super-capacitors.

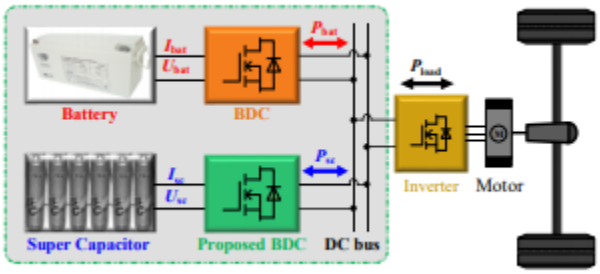


Fig. 19 Hybrid energy sources system of electric vehicles.

The experimental results of the bidirectional power flow control are shown in Fig. 20. Fig. 20(a) shows Ibat and Isc when the proposed bidirectional DC-DC converter (BDC) is operating (i.e. the DC bus is powered by the HESS). Fig. 20(b) shows Ibat and Isc when the proposed BDC is not operating (i.e. the DC bus is just powered by the battery). It can be seen from Fig. 20(a) that, when the DC bus power demand is changed from 400W to 650W with a step change, the control system sets the control signal Uc=0. At the same time, the proposed switched-capacitor bidirectional converter responds quickly and operates in the step-up mode. The current Isc quickly goes to 6A, and the instantaneous power provided by the super-capacitor is nearly equal to the required power change of the DC bus, avoiding any step change in current from the battery. Following this process, the current of the battery rises from 8A to 13A gradually, and the current of the super-capacitor falls to zero from Isc=6A to match the increase of the battery current. Similarly, when the DC bus demand power is changed from 650W to 400W with a step change, the control system sets the control signal Uc=1.

The proposed switched-capacitor bidirectional converter responds quickly and operates in the step-down mode. The current Isc quickly goes up to 6A with the opposite polarity. As a result, the current from the battery falls from 13A to 8A gradually, and the current of the super-capacitor falls to zero from Isc=-6A. If the proposed BDC is not operating, the battery has to supply all the load demands by itself. It can be seen from Fig. 20(b) that, when the DC bus demand power is changed from 400W to 650W with a step change, the current Ibat needs to suddenly increase from 8A to 13A with a step change. When the DC bus demand power is changed from 650W to 400W with a step change, the current Ibat suddenly decreases from 13A to 8A with a step change. Therefore, when the load power changes with a step, the output current of the battery also has to change instantaneously. This has a detrimental impact on the battery itself during the electric vehicle's acceleration and deceleration, as it shortens the battery's service life. Comparing the experimental results of Fig. 20 (a) and (b), it is seen that when the DC bus demand power suddenly increases or decreases, the proposed switched-capacitor bidirectional converter can respond quickly according to the control signal Uc, and the super-capacitor can compensate (take in or send out) the power difference between the battery and the DC bus side to ensure that the current from the battery changes slowly. Therefore the overall aim of improving the battery life can be achieved. The efficiencies of the proposed bidirectional DC-DC converter in the

step-up and step-down modes were measured using a YOKOGAWA/WT3000 power analyzer and are shown in Fig. 21, when the high-side voltage Uhigh is 300V and the low-side voltage Ulow varies from 40V to 100V or 100V to 40V continuously. According to Fig. 21, the measured efficiencies range from 90.08 to 94.39% in the step-up mode, and from 90.86% to 94.45% in the step-down mode. The efficiencies are improved when the low-side voltage Ulow increases (due to the lower voltage-gain), and the efficiency in the step-down mode is slightly higher than that in the step-up mode. Moreover, the maximum efficiencies are 94.39% and 94.45% for step-up and step-down modes respectively when the low-voltage side Ulow is 100V.

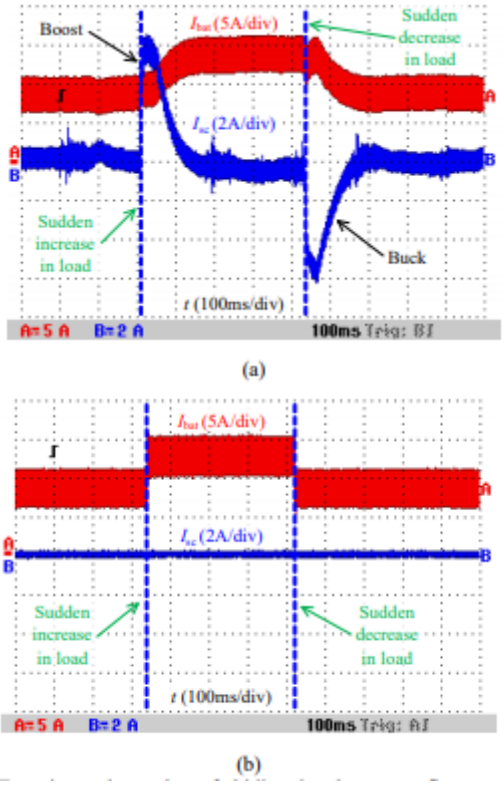


Fig. 20 Experimental results of bidirectional power flow control. (a) Super-capacitors are taken into operation. (b) Super-capacitors are not taken into operation.

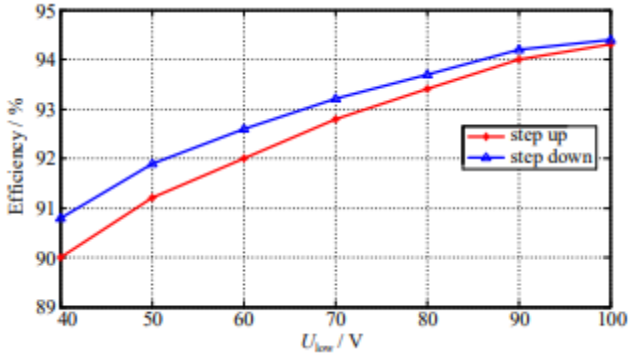


Fig. 21 Efficiencies of the proposed switched-capacitor bidirectional converter in step-up and step-down modes (U_{high}=300V, U_{low}=40V~100V, Pn=300W).

The calculated power loss distributions for the experiment when U_{low}=40V, U_{high}=300V and Pn=300W are shown in Fig. 14. In step-up mode, the total losses of the converter are 13.548W, and the loss distribution is shown in Fig. 22(a). By analyzing the power loss distributions, it can be concluded that

the major loss comes from the inductor, namely the copper and core losses of the inductor account for 38.566% of the total losses. The capacitor losses account for 22.018% of the total losses. The conduction and switching (turning on and off) losses of the semiconductors account for 19.922% and 19.494%, respectively. In step-down mode, the total losses of the converter are 12.508W, and Fig. 22(b) shows the power loss distributions. The largest power losses are also the copper and core losses of the inductor, which account for 41.774% of the total losses. The conduction losses and the switching (turning on and off) losses of the semiconductors account for 39.422%, and the remaining 18.804% of the total losses is occupied by the capacitor losses.

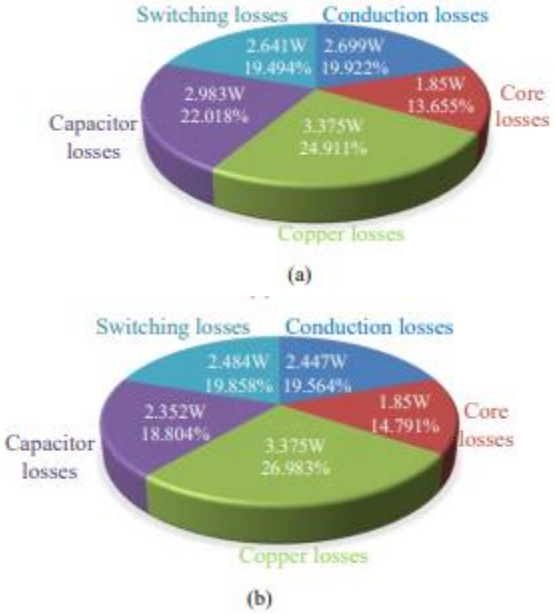


Fig. 22 Calculated power loss distributions for the experiment when U_{low}=40V, U_{high}=300V, and Pn=300W. (a) In step-up mode. (b) In step-down mode.

VI. CONCLUSIONS

A switched-capacitor bidirectional DC-DC converter has been proposed. The topology has a high step-up/step-down ratio and a wide voltage-gain range, in the case of requiring less number of components with the reduced voltage stress. The synchronous rectifiers can turn on and turn off using ZVS, and the efficiency is improved. The proposed bidirectional DC-DC converter, which interfaces the low voltage super-capacitor and the high voltage DC bus, can rapidly output or absorb the power difference due to a load step change. It can satisfy the requirements of a complex dynamic response, and effectively protect the battery from providing a step change in current. Thus, the proposed bidirectional DC-DC converter is suitable for the power interface between the low-voltage super-capacitors and the high-voltage DC bus of a HESS for electric vehicles.

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