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Design of Low Power, High Speed Fine Grain and Coarse Grain Double Tail Comparator

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***Abstract** : Comparator is a fundamental building block in ADCs. Comparator is a device that compares two voltages or currents and gives a digital output that indicates which of the input is larger. In design of ADCs, comparators of low power consumption, high speed are used. In high speed analog to digital converters, comparator design has a crucial influence on the overall performance that can be achieved.*

In this paper, we have proposed a new low power, high speed single tail and double tail comparators using power gating techniques. The comparison of speed and power consumed by proposed fine grain and coarse grain double tail comparators with traditional comparators like single tail and double tail comparators is also presented.

We observed that minimal propagation time delay and low power consumption is achieved by the proposed fine grain double tail comparators which make them suitable for high speed ADCs.

Index Terms–Course Grain Double tail comparator, Fine Grain single tail comparator, Fine Grain Double tail comparator, dynamic clocked comparator, high speed analog to digital converters, low power analog design, switching transistor , preamplifier based comparators.

I. Introduction

Over the years, development of digital integrated circuit has closely followed Moore's Law. As a result, transistor size has greatly shrunk and the speed of digital circuit has been exponentially increased. This trend, which still continues today, widens the gap between the digital circuit and its analog counterpart. In high-speed analog-to-digital converters, comparator design has a crucial influence on the overall performance that can be achieved. Comparator is widely used in the process of converting analog signals to digital signals. In the A/D conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal and it compare the analog signal with another reference signal and outputs are binary signal based on the comparison. Low power and high speed ADCs are the main building blocks in the front-end of a radio-frequency receiver in most of the modern telecommunication systems.

The preamplifier stage amplifies the input signal to improve the comparator sensitivity and isolate the input of the comparator from switching noise coming from positive feedback stage. The latch stage is used to determine which of the input signals is larger and extremely amplifies their difference. The output buffer amplifies the information from latch and gives digital signal as output. The latched comparator is used for the clock signal and indicates digital output level; whether its differential input signal is positive or negative. A positive feedback mechanism to regenerate the analog input signal into a full scale digital signal is much faster and power efficient than performing multi-stage linear applications.

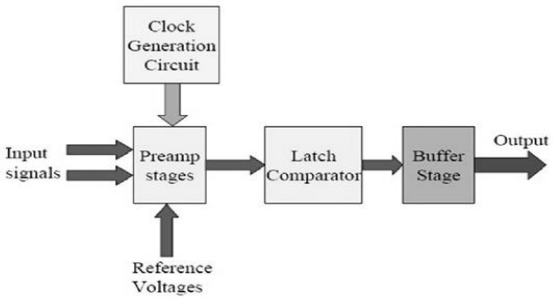


Figure 1: Comparator Architecture

The preamplifier latched comparator consists of an amplifier and a latch. The amplifier which is added before the latch can reduce offset voltage to obtain a high resolution. This type of latched comparator was also used for high speed and low power performance. Input-offset voltage is a difficult problem in comparator design. In precision applications, such as high-resolution converters, large input-offset voltages cannot be tolerated. Fully dynamic latched comparator achieves low power dissipation but also improves kickback noise and reduces the clock driving requirement compared with a conventional comparator. So these comparators are most widely used in high speed ADCs

Ii. Coarse Grain Double Tail Comparator

As long as fn continuously falling, the corresponding PMOS control transistors (Mc1 in this case) starts to turn on, pulling fp nodes back to the VDD; so another control transistors (Mc2) remains off, allowing fn to be discharged completely. In other words unlike conventional double tail dynamic comparators which in Vfn/fp is just functions of input transistors transconductance of input voltage difference in the proposed structures as soon as the comparator detects for the instance nodes fn discharging faster, a PMOS transistors (Mc1) turns on, pulling the other nodes fp back to the VDD. Therefore, the time passing, the difference between the fn and fp (Vfn/fp) increases in a exponential manner, leading to the reductions of latch regeneration times.
The comparator with the coarse grain power gating technique is shown in the figure 2

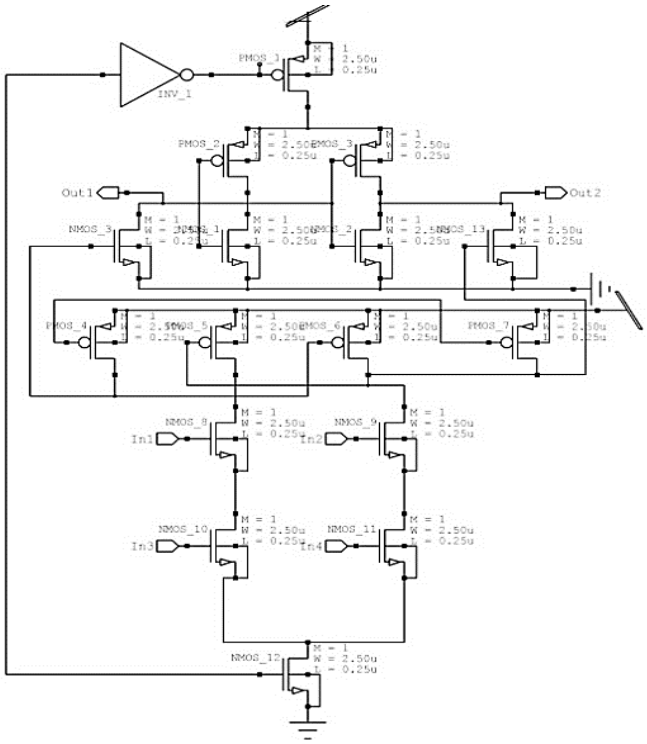


Figure 2: Coarse Grain Double Tail Comparator

In this evident that the double tail comparator technologies can operates faster and be used in lower supply voltages, while consuming nearly the same powers as the conventional dynamics comparator. In case of even much better for the proposed comparator when compared to the conventional double tail topology.

III. Fine Grain Single Tail Comparator

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 3.
The operation of the comparator is as follows. During the reset phase when CLK=0 and Mtail is off, reset transistors (M7–M8) pull both output nodes Outnand

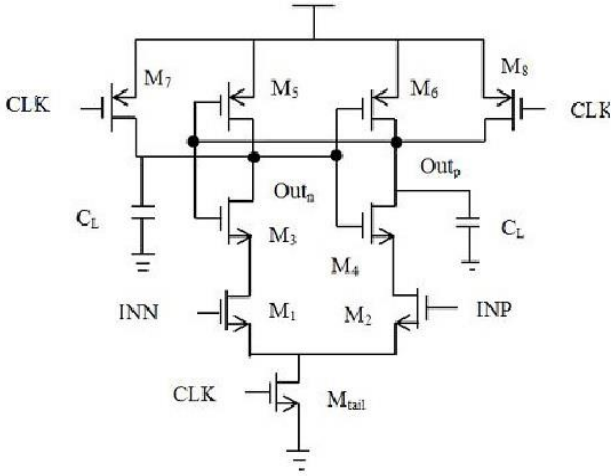


Figure 3: Fine Grain Single Tail Comparator

Out_p to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK=VDD, transistors M7 andM8 are off, and Mtail is on. Output voltages (Out_p, Out_n), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP >VINN, Out_p discharges faster than Out_n, hence when Out_p (discharged by transistor M2 drain current), falls down to VDD–|Vthp | before Outn (discharged by transistor M1 drain current), the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5 and M4, M6).

Thus, Out_n pulls to VDD and Out_p discharges to ground. If VINP <VINN, the circuits works vice versa. The delay of this comparator is comprised of two time delays, t0andtlatch. The delay t0represents the capacitive discharge of the load capacitance CL until the first p-channel transistor (M5/M6) turns on. In case, the voltage at node INP is bigger than INN (i.e.,VINP>VINN), the drain current of transistor M2 (I2) causes faster discharge of Out_{pnode} compared to the Out_{nnode}, which is driven by M1 with smaller current.

The total delay is directly proportional to the comparator load capacitance CL and inversely proportional to the input difference voltage (Vin). Besides, the delay depends indirectly to the input common-mode voltage (Vcm). By reducing Vcm, the delay t0 of the first sensing phase increases because lower Vcm causes smaller bias current (Itail).On the other hand, (4) shows that a delayed discharge with smaller Itail results in an increased initial voltage difference (V0), reducing tlatch. Simulation results show that the effect of reducing the Vcm on increasing of t0 and reducing off latch will finally lead to an increase in the total delay. It has been shown that an input common-mode voltage of 70% of the supply voltage is optimal regarding speed and yield.

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistorsM3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5 or M6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistorsM3andM4, where the gate source voltage of M5 and M6 is also small; thus, the delay time of the latch becomes large due to lower transconductance.

Another important drawback of this structure is that there is only one current path, via tail transistor M tail, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better Gm/I ratio, a. large tail current would be desirable to enable fast regeneration in

the latch. Besides, as far as Mtail operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favourable for regeneration.

IV. Proposed Fine Grain Double Tail Comparator

As long as fn continuously falling, the corresponding PMOS control transistors (Mc1 in this case) starts to turn on, pulling fp nodes back to the VDD; so another control transistors (Mc2) remains off, allowing fn to be discharged completely. In other words unlike conventional double tail dynamic comparators which in Vfn/fp is just a functions of input transistors transconductance of input voltage difference in the proposed structures as soon as the comparator detects for the instance nodes fn discharging faster, a PMOS transistors (Mc1) turns on, pulling the other nodes fp back to the VDD.

Fig. 4 demonstrates the schematic diagram of the proposed dynamic double tail comparator. Due to the better performance of double-tail architecture in low voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase Vfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a crosscoupled manner.

During reset phase (CLK=0, Mtail1 andMtail2 are off, avoiding static power), M3andM4pulls both fn and fp nodes to VDD,

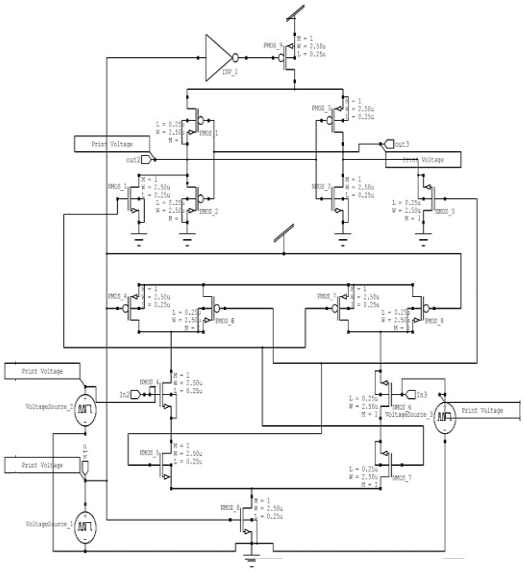


Figure 4: Fine Grain Double Tail Comparator

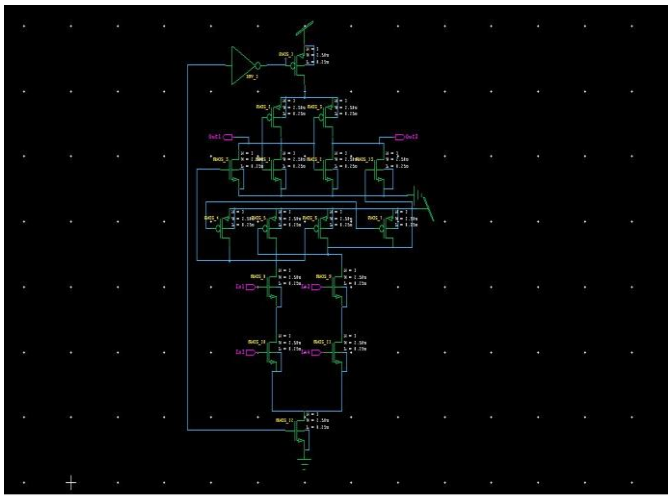
hence transistor Mc1andMc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision-making phase (CLK=VDD, Mtail1 and Mtail2 are on), transistorsM3andM4turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP >VINN, thus fn drops faster than fp, (since M2provides more current thanM1).

As long as fn continues falling, the corresponding pMOS control transistor (Mc1in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which Vfn/fp is just a function of input transistor transconductance and input voltage difference (9), in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD. Therefore, by the time passing, the difference between fn and fp

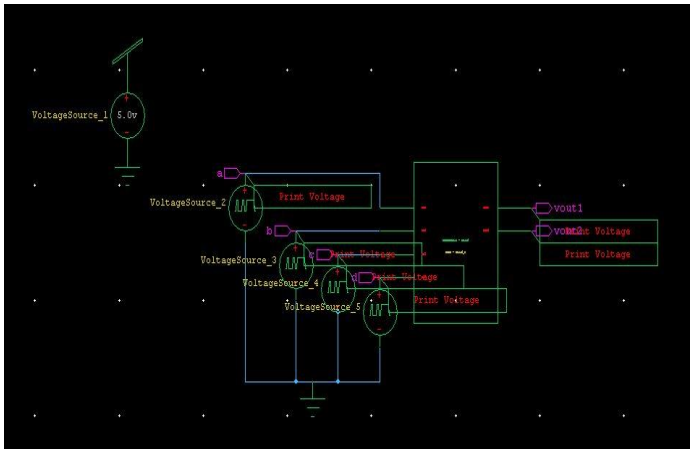
(Vfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g.,Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, andMtail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors.

At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to VDD (during the reset phase), both switches are closed and fn and fp tart to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference.

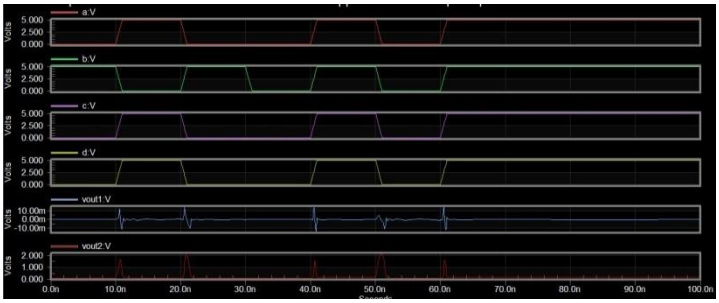
V. Simulation Results



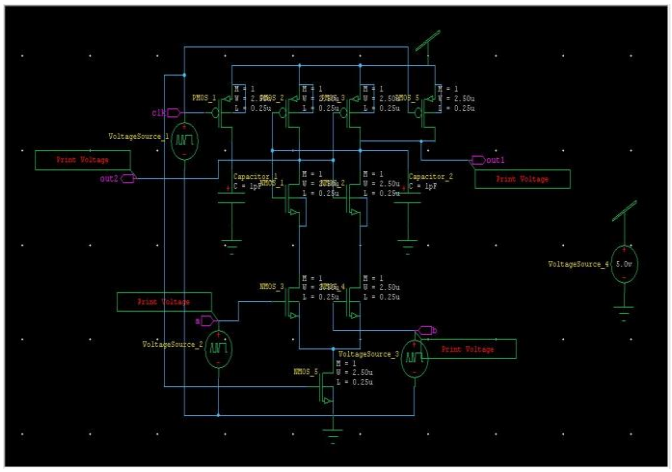
Layout Design of Coarse Grain Double Tail Comparator



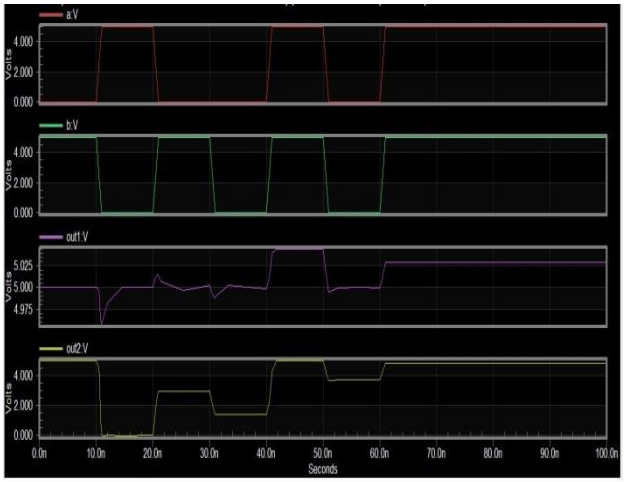
Extension Schematic of Coarse Grain Double Tail Comparator



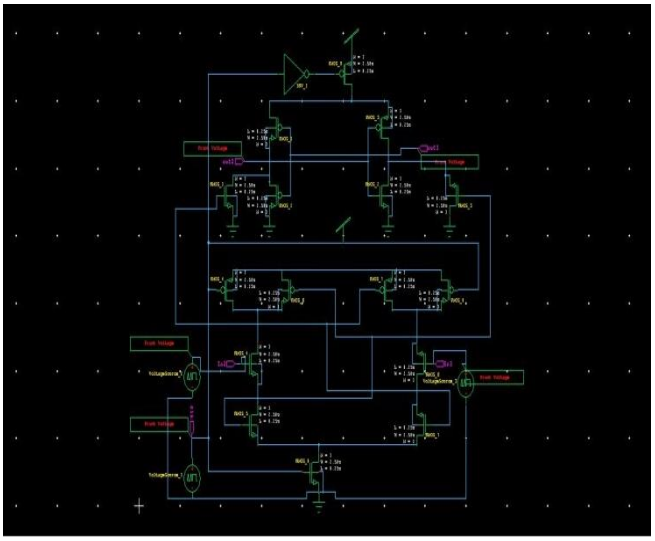
Simulation of Coarse Grain Double Tail Comparator



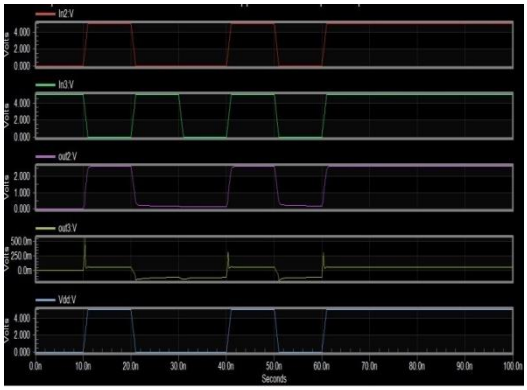
Schematic of Fine Grain single Tail Comparator



Simulation of Fine Grain single Tail Comparator



Proposed Schematic of Fine Grain Double Tail Comparator



Simulation of Fine Grain Double Tail Comparator

VI. Performance Analysis & Conclusion

The comparator circuits are mainly optimized for the low propagation time, minimal input referred offset voltage, low power consumption and minimal circuit area.The proposed fine grain double tail comparator, which shows low power consumption and low propagation time.

Parameter	**Coarse Grain Double Tail**	**Fine Grain**	
		Single Tail	**Double Tail**
No of Transistors	18	9	19
Delay	80.9000ns	80.9000ns	50.9000ns
Power	9.10836 µW	8.909175 µW	4.1955 µW

Table: Illustrates the all the performance parameters of different comparators.

The minimal propagation time delay of 50ns, and power consumption of 4.19 µW is achieved by the proposed fine grain double tail comparator. These results show that power has been reduced. Thus proposed comparator is optimized in such a way that it shows low power and low input propagation time, which is suitable for high speed ADCs.

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