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Simulation of 11 Level Hybrid Cascade-Stack (HCS) Inverter with Reduced Number of Switches

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Abstract : *This paper presents a new multilevel topology based on cascaded hybrid multi-level (HCS) inverter. There are different topologies for cascaded inverters for reducing the switches, power loss. The output voltage is increased and the number of switches is reduced with the HCS inverter. Due to this reduction in number of on-state switches, power loss and voltage drop is reduced. Simulation results for 11 level symmetric form of converter is described.*

Keywords –*Inverter, Switches, Leg-Inv, Cascade stack*

I. INTRODUCTION

The development in the multilevel inverters for industry applications are increased today. The main use of multilevel concept is to generate pure sinusoidal output signal with the help of dc link voltage. The concept of multilevel inverters are classified in three configurations namely (a) diode clamped, (b) flying capacitors and (c) cascaded type multilevel inverter. In case of diode clamped inverter it is not possible to obtain the balanced voltages. Flying-capacitor inverters are used for medium voltages and have the advantages like equal voltage stress on power switches, self balancing of capacitors and no need for a transformer. Cascade multilevel inverter is designed by a series of half bridge, full bridge and other sources. General type cascaded multilevel inverter is formed from H-Bridge units. H- Bridge consists of 4 switches in which pair of switches are operated in a complementary fashion. Each inverter consists of a DC source that produces zero, positive and negative voltages at its output terminal. H- Bridge consists of 4 switches. The proposed multilevel hybrid cascaded-stack (HCS) is shown in figure 2. HCS is composed of four switches and two equal amplitude DC sources. In order to avoid the undesirable conduction of a middle switch a directional switch is used in each unit.

II. COMPARISION STUDY

Figure 3 shows the configuration structure for HCS topology and from this system the output voltage generated is $2V_n$ for n^{th} unit.

The range of voltages under symmetric configuration is expressed as:

$$Vi = V1;\ i = 1,2, \ldots.n \quad (1)$$

The output voltage obtained from the each basic unit is in terms of $2V_1$. Therefore, the output from the n^{th} unit is expressed as,

$$V(n) = (4n - 1)\,V1 \quad (2)$$

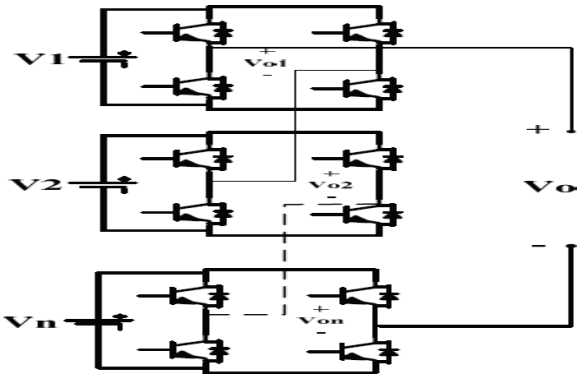

Fig 1. Cascaded H-bridge multilevel converter.

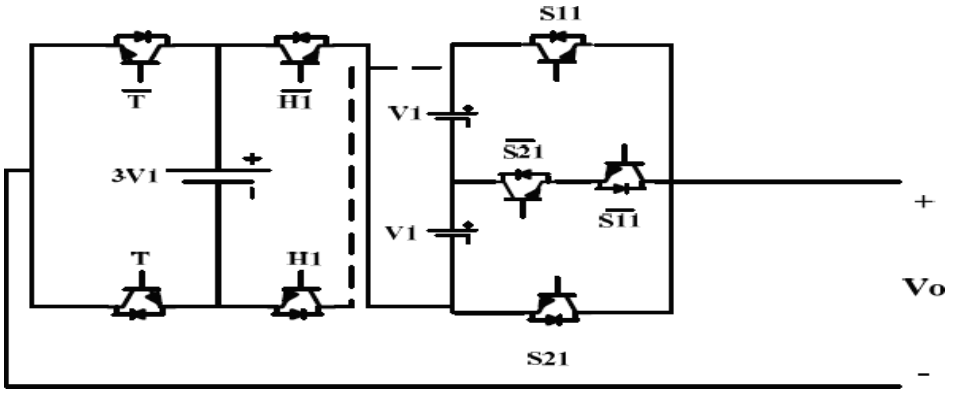

Fig 2. Proposed HCS topology under single basic unit.

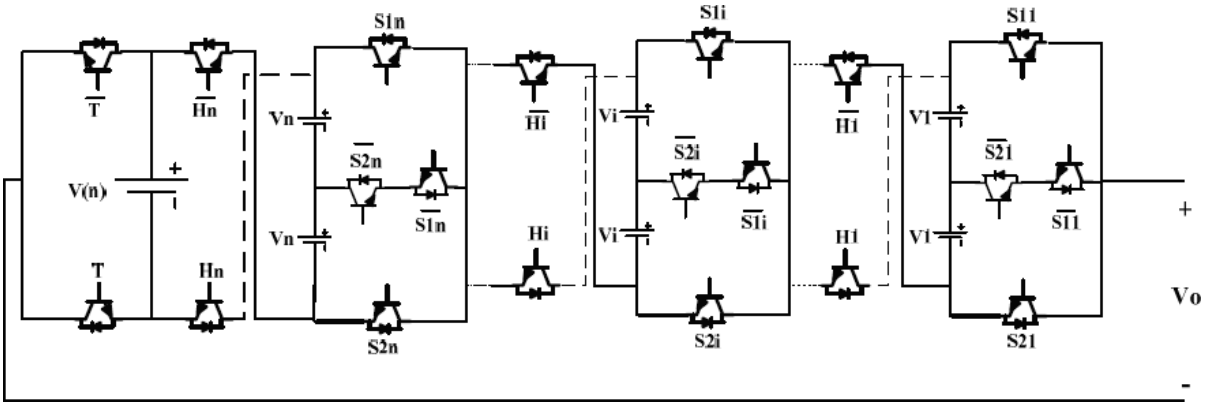

Fig 3. Proposed HCS Converter.

The essential unit displayed in Figure 2 in the symmetric arrangement delivers a 11-level voltage waveform. Its exchanging states are represented in Table 1. In view of this table, the operational rule of the HC-S multilevel inverter will be a great deal more intelligible. The center bidirectional switch works in a reciprocal way with two IGBTs on the top and base of the essential unit. Hence, it is \on" when the finish and base IGBTs are off.

Table 1. Switching states of the 11-level symmetric proposed topology.

State no.	Switching state				V_o	I_o
	S_{11}	S_{21}	H_1	T		
1	1	0	0	1	$+5V_1$	+
2	0	0	0	1	$+4V_1$	+
3	0	1	0	1	$+3V_1$	+
4	1	0	0	0	$+2V_1$	+
5	0	0	0	0	$+V_1$	+
6	0	1	0	0	0	
7	0	0	1	1	$-V_1$	−
8	0	1	1	1	$-2V_1$	−
9	1	0	1	1	$-3V_1$	−
10	0	0	1	0	$-4V_1$	−
11	0	1	1	0	$-5V_1$	−

The DC voltage wellsprings of the HCS Inverter and the customary course inverter are equivalent numerically, and equivalent to 2n + 1, where n is the no. of units. In some investigation, correlations are done by number of bidirectional switches rather than the quantity of IGBTs, which brought about more prominent lessening of number of switches. Along these lines, it is not precise examination.

The number of switches and Peak Inverse Voltage (PIV) in the proposed system is obtained as follows:

$N_{switches} = (m/2) + (5/2)$ *(4)*

*Peak inverse Voltage (PIV) = (13/6)*m + (37/6)* *(5)*

Table 2 Comparison of conventional cascaded multilevel inverter and Proposed HCS Inverter

Sources	Conventional Method	Proposed Method
DC Sources	2n+1	2n+1
Switches	8n+4	6n+2
Output Levels	12n+3	12n-1
V_{max}	6n+1	6n-1
Peak Inverse Voltage	20n+4	26n-4
On-State Switches	4n+2	3n+1

III. SWITCHING POWER LOSSES

In general the losses in the proposed system are in 2 types:

1. IGBT switching losses
2. Power Loss in antiparallel diode

The power loss in the IGBT is given by

$P_{IGBT,\,s} = (E_{on,s} + E_{off,s}) f_{IGBT}$ *(6)*

Where, $P_{IGBT,\,s}$ – *Switching Power Loss in IGBT*
$E_{on,s}$ – *Turn on loss in IGBT*
$E_{off,s}$ – *Turn off loss in IGBT*
f_{IGBT} – *switching frequency*

The power loss in antiparallel diode is given by,

$P_{anti\_D,} = (E_{on,anti\_D} + E_{off,anti\_D}) f_{IGBT}$ *(7)*

The conduction power loss rely upon upon the quantity of moves, and they are affected by the adjustment strategy. At long last, the aggregate conduction power loss can be figured as takes after:

$$P_{IGBT} = \sum_{i=1}^{n} P_{IGBT,Si} + P_{IGBT,anti\_Di} \quad (8)$$

Where *n* is determined by the switching pattern and indicates the number of turned-on IGBTs.

IV. SIMULATION RESULTS

Figure 4 illustrates the simulation results for 11 Level proposed HCS inverter. The simulation results for output voltage and current and its phase difference is shown in figure 4

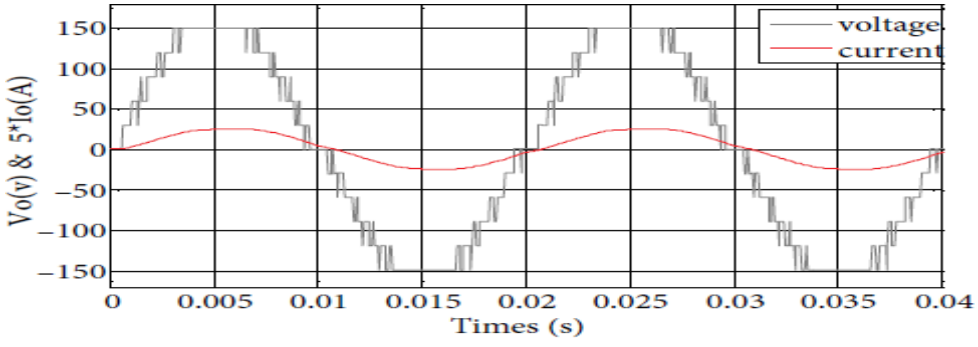

Fig 4: Waveform for output voltage and current for HCS converter

V. CONCLUSION

In this paper, a new multilevel topology based on multilevel hybrid cascade-stack (HCS) inverter, which is obtained by the series connected modules. This topology is compared with other topologies and it is shown that the number of active switches are reduced which reduces the voltage drop. The future work for this topology is extended to the 23 level and 31-Level symmetric and asymmetric modes which improves the THD of the output voltage.

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