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Topology With BoostFacility

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Abstract : *A new switched capacitor inverter topology suitable for photovoltaic applications is proposed in this paper. The inverter is capable of boosting up low voltage DC in to high voltage DC and then invert it to the required voltage level with high quality in single stage. The proposed inverter has a special extended structure, which minimizes the number of components and devices when compared to the conventional multilevel inverter topology. Further some of the switches in the topology operate in the low frequency and this result in reduction in switching losses there by increasing the efficiency. The inverter is switched by the means of level shifting carrier based Pulse Width Modulation (PWM) methodology which maintains the capacitor voltages at a balanced level. The proposed topology operation is verified through simulation in MATLAB/SIMULINK and the results are presented. A detailed comparison of the proposed inverter with other inverter proposed in the literature is also presented*

Keywords - *Switched Capacitor, Multilevel inverter, Voltage balancing in capacitors, Level shifted PWM technique*

I. INTRODUCTION

In recent days, multilevel inverter (MLIs) has grown to be an attractive topic among researches, who work in the area of which includes Renewable energy integration and high power converters etc. MLIs are capable of generating nearly sinusoidal waveforms, which improves the problem of power quality. Principally, MLIs produces a high quality AC voltage waveform from a several DC voltage sources. In general MLIs are classified into three different categories they are: Cascaded H bridge inverter topology, diode clamped inverter topology and capacitor clamped inverter topology. The main disadvantage of diode clamped inverter topology is that it shares unequal voltage between series connected capacitors and also it requires many diodes to produce more number of voltage levels at the output. Some of the advanced diode clamped inverter topologies are presented in [1]-[4]. In those topologies diodes are replaced with active devices, but this result in increased conduction losses because of high total conduction voltage at zero vectors. A cascaded MLI has many H bridges connected in series. Each H Bridge requires a separated DC source. If the magnitude of DC sources of all the H Bridge is equal then the configuration is called as symmetrical configuration, where as if the magnitudes of DC sources are different then the configuration is called as Asymmetrical configuration.
Asymmetrical configuration can generate more number

of levels at the load when compared to Symmetrical configuration. But controlling the asymmetrical configuration is highly complicated when compared to symmetrical configuration. Further in both the configurations the number of DC source and the number of devices is higher for higher levels.

Photovoltaic (PV) applications, generally requires a DC-DC boost converter to step up a low DC voltage into a high DC voltage as required by the grid or the standalone load. This high DC voltage is again inverted in to AC voltage using a high quality MLI. Thus it requires two stages of conversion. First stage is to step up the low voltage DC of PV in to high voltage and the second stage is to convert the high DC voltage generated from first stage into AC voltage of high quality. Thus this two stage conversion increases the system complexity and reduces the efficiency of the system.

This paper proposes a new extendable capacitor clamped MLI using switched capacitor topology. Further the proposed inverter uses a level shifting carrier based Pulse Width Modulation method to trigger the devices of the inverter. The main advantage of the proposed inverter is that the number of components used is minimized due to its combined structure. Further the proposed inverter can be extended to any required number of levels just by adding four switches and four capacitors. The remaining part of the paper is organized as follows. Topology derivation is derived in section II. In section III PWM topology for capacitor voltage balancing is dealt in detail. Finally, simulation results are detailed in Section III.

PROPOSED TOPOLOGY

The proposed topology is shown in figure 1, which consists of conventional H bridge and a switched capacitor network connected to the front end of the conventional H bridge. The switched capacitor topology (SCT) is proposed in [5]-[8] as shown in figure 1 in dotted structure. The SCT has four capacitors and eight power devices. Switches S_1, S_4, S_{1B}, S_{2A} are named as S_P switches and S_2, S_3, S_{1A}, $S_{2B}$are named as S_N switches. The operation of the proposed inverter has two states. In state A S_P switches are turned ON and in state B S_N switches are turned ON as shown in figure 2(a) and 2(b) respectively.

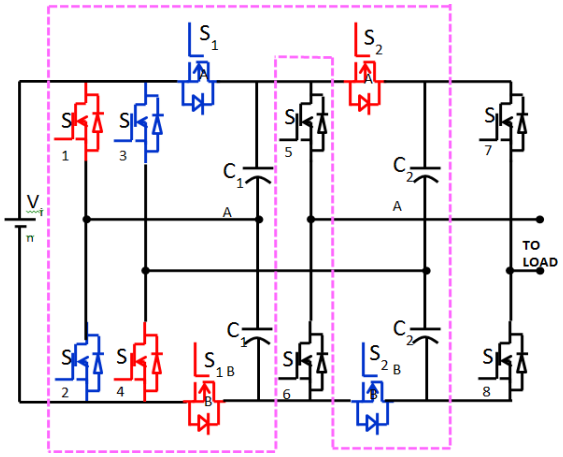

Fig 1. Proposed Inverter

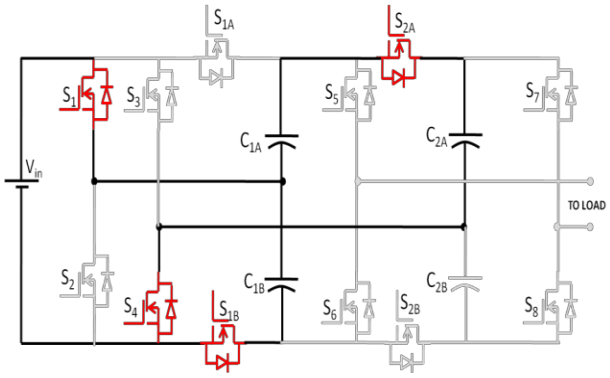

Fig 2(a)

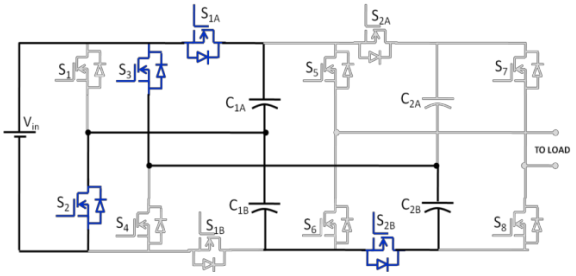

Fig 2 (a) Conduction Diagram for State A (b) Conduction Diagram for State B

There are five modes of operation of the proposed inverter to generated five levels. Operating modes of the proposed inverter are shown in figure 3 and explanations are given for each mode. Mode 1: Figure 3(a) and figure 3(b) shows the mode 1 operation, in mode 1 S_P group switches and S_5 and S_7 switches are in ON condition and the other switches are in OFF condition. Output voltage across the load is 0 volts since the input voltage is not connected to the load. Capacitor C_1 and C_{2A} are in parallel to each other. Similarly when switches of S_N group and S_6 and S_8 are in ON condition a similar situation exists.

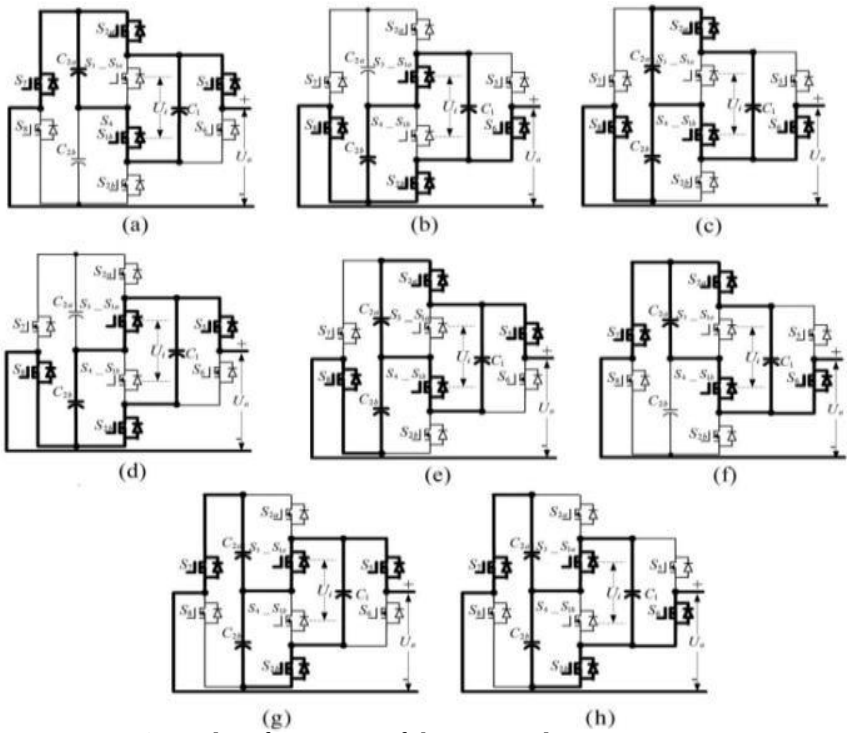

Fig 3. Modes of operation of the proposed inverter.

Mode 2: In Fig. 3(c) and 3(d), corresponds to mode 2, voltage value of $2V_{in}$can be obtained from the proposed converter. One operation state is that switches group S_P, switches S_6, S_8 are turned ON and other switches are turned OFF, capacitors C_1 and $C_{2a}$are in parallel connection, inverter has the output voltage of C_{2b}, as shown in Fig. 3(c). Fig. 3(d)shows another operation state with switches group S_N, switchesS_5, S_8 turned ON and other switches turned OFF, capacitors $C_1$and $C_{2b}$are in parallel connection, the inverter produces the voltage of C_{2b}.

Mode 3: In Fig. 3(e), corresponds to the mode 3 operation in this, switches group S_P, switches S_5, S_8 become on-state, capacitors C_1 and$C_{2a}$are parallel connection, the inverter outputs the summation voltage of capacitor $C_{2a}$and C_2.

Mode 4: In Fig. 3(f) and 3(g) corresponds to the mode 4 operation, switches group S_P, switches S_6, S_7 are turned ON and capacitors C_1 and$C_{2a}$are in parallel connection, the inverter outputs the reverse voltage of $C_{2A}$with value of $-V_{in}$. In Fig. 3(g), switches group S_N, switches S_5, S_7 conduct and capacitorsC_1 and $C_{2B}$are in parallel connection, the inverter outputs the reverse voltage of $C_{2A}$with value of $-2V_{in}$.

Mode 5: In Fig. 3(h), corresponds to mode 5 operation, switch group S_N, switches S_6, S_7 become on-state and capacitors $C_1$and $C_{2B}$are in parallel connection, the inverter produces the reverse voltage of $C_{2A}$and $C_{2B}$with value of $-4V_{in}$.

PERFORMANCE COMPARISION

The performance of the proposed inverter is compared in terms of active devices, diodes, capacitors, front end boost conversion, voltage stress, switching frequency, capacitor voltage balance control and number of DC sources with that of other similar type of inverters available in the literature. Table 1 shows a detailed comparison.

SWITCHING LOGIC

The switching logic of the proposed inverter is shown in figure 4. It has four level shifted carrier waveforms compared with the sinusoidal reference waveform.From figure 4 it can be seen that four switches operates at low frequency which reduces the switching losses there by increasing the efficiency. Table 2 shows the switching logic of the proposed inverter in a simplified form.

II. FIGURES AND TABLES

	Five Level Inverter			
	Diode Clamped	Capacitor Clamped	Cascaded H bridge	Proposed Inverter
Active Switches	8	8	8	12
Diodes	12	0	0	0
Capacitors	4	10	2	4
Front End Boost Conversion	Needed	Needed	Needed	Not Needed
Voltage Stress	0.25 U_B	0.25 U_B	0.5 U_B	✓ 0.25 U_B (8 Nos) ✓ 0.5 U_B (2 Nos) ✓ U_B (2 Nos)
Switching Frequency	f_c	f_c	f_c	f_c (4 switches) f_l (4 switches)
Capacitor Voltage Balance Control	Difficult [9]	Difficult[10]	Difficult	Easy
Number of DC sources	1	1	2	1

Table 1: Performance Comparison

Condition for Modulation and Carrier Wave		Switching States					
		S_P	S_N	S_5	S_6	S_7	S_8
$U_S >= U_C$	$U_S >= U_A$	1	0	1	0	0	1
	$U_S < U_A$	0	1				
$0 <= U_S < U_C$	$U_S >= U_B$	1	0	0	1	0	1
	$U_S < U_B$	0	1				
$-U_C <= U_S < 0$	$U_S >= U_C$	1	0	1	0	1	0
	$U_S < U_C$	0	1				
$U_S < -U_C$	$U_S >= U_D$	1	0	0	1	1	0
	$U_S < U_D$	0	1				

Table 2: Switching Logic of the proposed inverter.

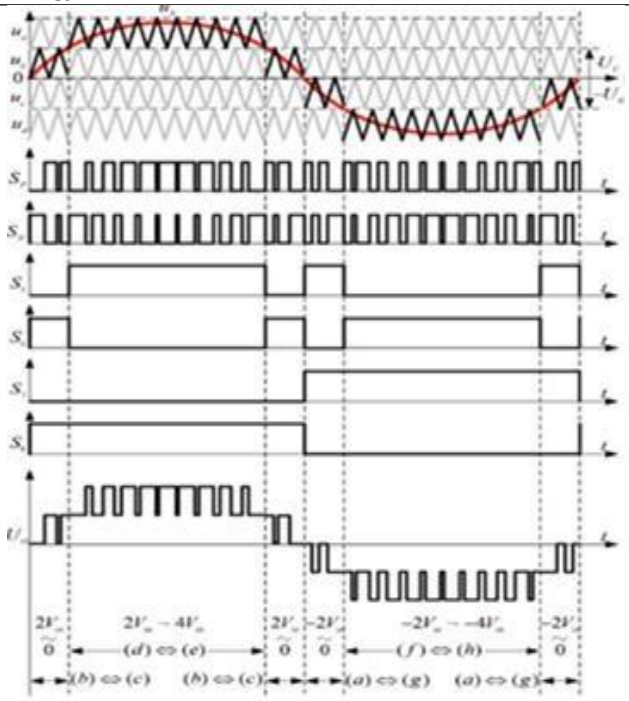

Figure 4 Switching logic of the proposed inverter.

III. SIMULATION RESULTS

A conclusion section must be included and should indicate clearly the advantages, limitations, and possible applications of the paper. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

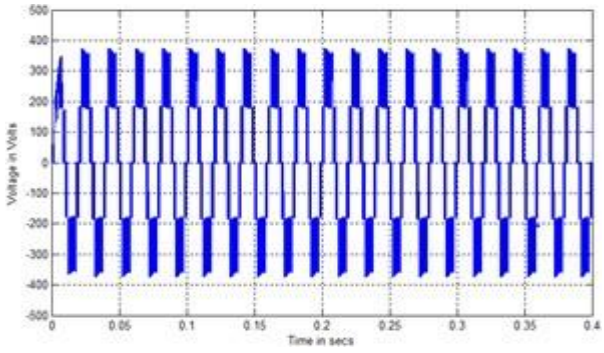

Fig 5. Load Voltage Waveform

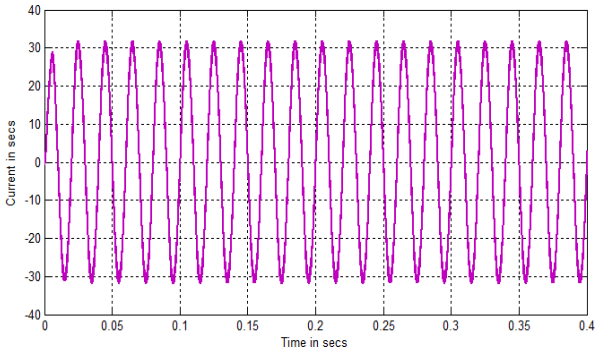

Fig 6. Load Current Waveform

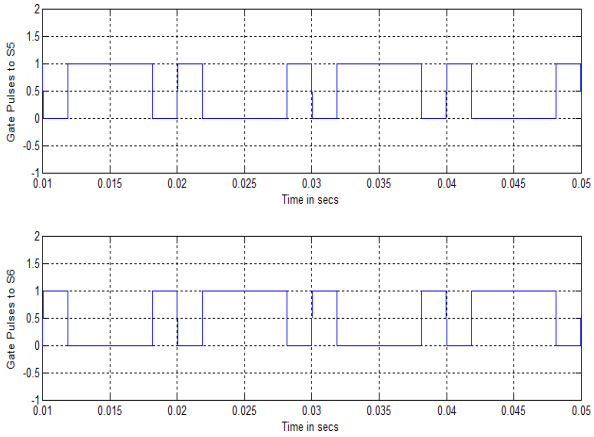

Fig 7 Switching pulses for S_P and S_N Switches.

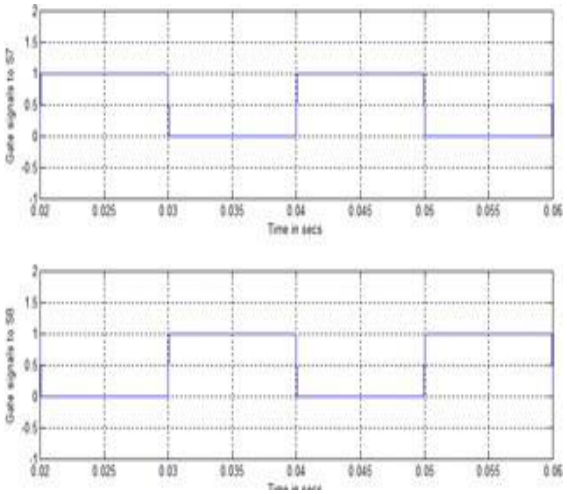

Fig 8Switching pulses for S_5 and S_6 Switches

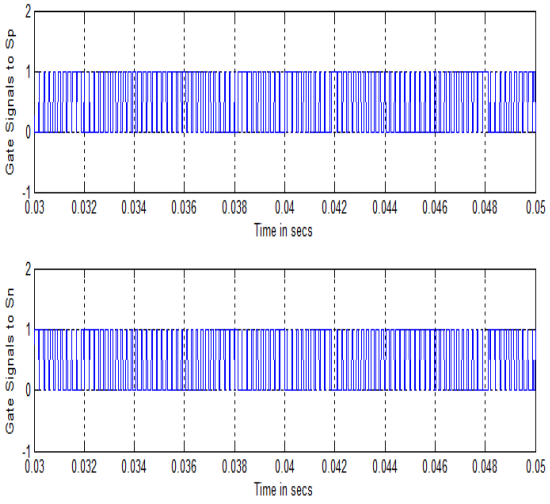

Fig 9 Switching pulses for S_7 and S_8 Switches

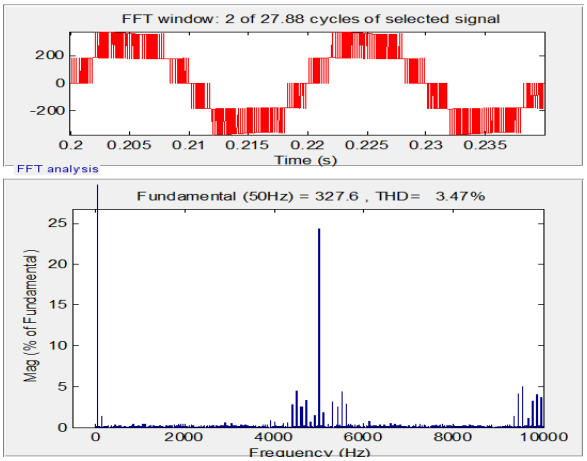

Fig 10 Output Voltage THD

The total harmonic distortion of the inverter when it is operating in full load is shown in figure 10.The modulation index of the proposed inverter is varied from 0 to 1 and the performance of the inverter is studied. It is found that the number of levels reduces to three when the modulation index is reduced. The voltage waveform of the reduced modulation index is shown in figure 11. Figure 12 shows the current waveform for modulation index of 0.5. It is found that the total harmonic distortion is less than 5% which is the prescribed limit of IEEE standards.

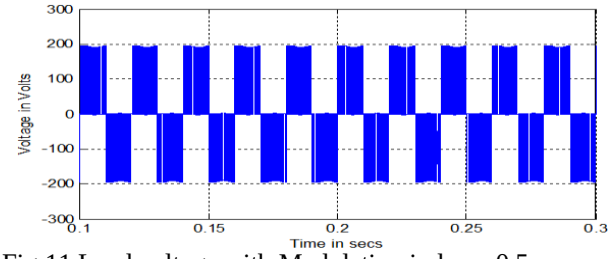

Fig 11 Load voltage with Modulation index = 0.5

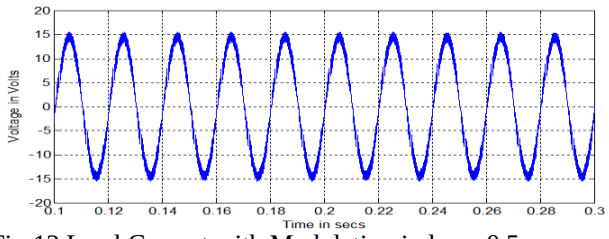

Fig 12 Load Current with Modulation index = 0.5

IV. CONCLUSION

A novel single phase five level boost inverter is presented which is suitable for renewable energy applications. Some of the switches of the proposed inverter operate in low frequency which makes the inverter to operate at high efficiency. The proposed inverter uses minimum number of switching devices when compared to the other inverters proposed in the literature. Simulation results are presented for different modulation indexes.

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