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Design of DPLL Using Sub-Micron 45 nm CMOS Technology and Implementation Using Microwind 3.1 Software

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Abstract : *Digital Phase locked loop (DPLL) is one of the most important devices in almost all the electronic systems. This paper introduces the design of DPLL using sub-micron 45nm CMOS technology and implemented using microwind 3.1 software. The Software microwind 3.1 is used to design and simulate an integrated circuit at physical description level. The performance of DPLL is also observed for the different variable input frequencies and result is observed up to the mark. The lock range for the DPLL and lock time is was also observed as expected.*

Keywords - *DPLL, 45 nm CMOS Technology, Microwind, power, frequency*

I. INTRODUCTION

A phase-locked loop or phase lock loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. While there are several differing types, it is easy to initially visualize as an electronic circuit consisting of a variable frequency oscillator and a phase detector [1]. The oscillator generates a periodic signal, and the phase detector compares the phase of that signal with the phase of the input periodic signal, adjusting the oscillator to keep the phases matched. Bringing the output signal back toward the input signal for comparison is called a feedback loop since the output is "fed back" toward the input forming a loop [1, 2].

Keeping the input and output phase in lock step also implies keeping the input and output frequencies are same. Consequently, in addition to synchronizing signals, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency. These properties are used for computer clock synchronization, demodulation, and frequency synthesis. Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications [3]. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many gigahertzes [4].

Mainly there are two types PLL as Analog and Digital PLL:

1. Analog PLLs are extensively used in communication systems as they maintain a linear relationship between the input and the output.
2. Digital PLLs are suitable for synchronization of digital signals, clock recovery from encoded digital data streams and other digital applications.

Phase Locked Loop mechanism implemented as either analog or digital circuits. Both implementations use the same basic structure. Both analog and digital PLL circuits include four basic elements

1. Phase Detector (PD) - This is a non linear device whose output contains the phase difference between the two oscillating input signals.
2. Loop Filter (LF) - The PLL filter is needed to remove any unwanted high frequency components which might pass out of the phase detector and appear in the VCO tune line. The loop filter is used to improve the performance of the PLL.
3. Voltage Controlled Oscillator (VCO) – This is another nonlinear device which produces an oscillation whose frequency is controlled by a lower frequency input voltage [6].
4. Feedback Path

The block diagram of simple PLL is shown in figure 1 consisting of Phase detector, Low pass filter and voltage controlled oscillator.

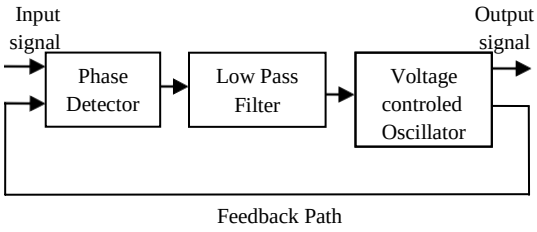

Figure 1.Block Diagram of PLL

II. LITERATURE SURVEY

Many researchers have given contributions towards Phase locked loop. The researchers' contributions towards PLL are discussed below;

Fleura Hajilou et al. (2015) proposed power supply isolation technique by employing a phase locked loop to de-correlate power supply from the crypto-processor block [7]. Feiran Lei et al. (2016) proposes a modified phase-locked synchronous oscillator to improve noise performance and locking behavior [8]. Mr. Vishwanath Muddi et al. (2015), designed current starved voltage controlled oscillator for PLL and implement using Cadence [9]. V. Nagarajan, B. Raju, (2016), designed charge-pump boost converter with PLL using compensator techniques [10]. Bhavana Goyal et al. (2016), designed charge pump PLL using improved performance ring VCO, which shows better performance in terms of power consumption, tuning range [11]. Purushothama Chary P, and et.al. (2015), proposes PLL for ZigBee application [12]. Gande Bhargav et al. (2016), designed PLL in 90 nm CMOS technology and implement using cadence [13]. Ping-Hsuan Hsieh et al. (2010), proposes PLL for GHz clock generation in large digital systems uses 65 nm CMOS technology [14]. Ward S. Titus and et al. proposes 5.6 GHz to 11.5 GHz DCO for Digital Dual Loop CDRs for PLL [15]. Delvadiya Harikrushna et al. [16], designed PLL with PFD using 45 nm CMOS technology. After meticulous study of the above work it observed that there is a scope for improvement to reduce the power consumption at different frequencies and different voltages which is implemented in this paper. The Software microwind 3.1 is used to design and simulate an integrated circuit at physical description level.

III. DESIGN OF PLL

For the design of DPLL XOR as phase detector is chosen as it requires less number of transistors compare to other types of phase detectors [17, 18] and it is shown in figure 2. The XOR gate as shown in figure 3 and its implementation using CMOS technology is shown in figure 4. The XOR gate output produces a regular square oscillation V_{PD} when two inputs have one quarter of period shift (90^0 or $\pi/2$). When the phase between two inputs of the phase detector is around π /2, V_{PD} is $V_{DD}/2$. Then it is increases up to V_{DD}. The gain of the phase detector is the ratio between V_{PD} and $\Delta\phi$. When the phase difference is larger than π, the slope sign is negative until 2 π, [1] shown in figure 5. When locked, then phase difference should be close to π /2.
Consequently, V_{PD} and the phase difference are linked by expression

$Gain(PD) = \frac{V_{PD}}{\Delta\phi}$	(1)
$\frac{V_{PD}}{\Delta\phi} = \frac{V_{DD}/2}{\pi/2}$	(2)
$= \frac{V_{DD}}{\pi}$	
$\therefore V_{PD} = \frac{V_{DD}}{\pi} \cdot \Delta\phi$	(3)

Where V_{DD}=0.9V and $\Delta\phi = \pi/2$

$$V_{PD} = \frac{0.9}{\pi} \cdot \frac{\pi}{2}$$
$$V_{PD} = 0.45V$$

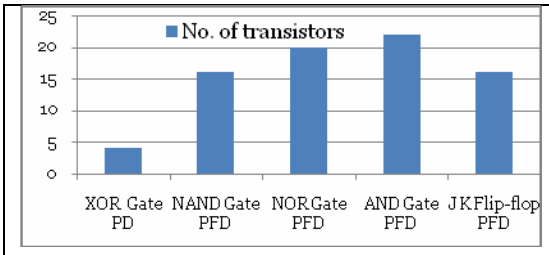

Figure 2: Types of phase detectors vs no. of transistors

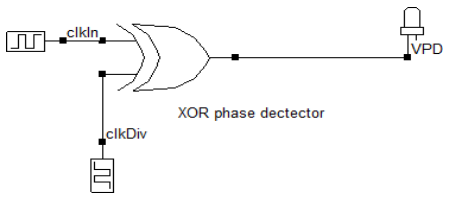

Figure 3. XOR Symbol

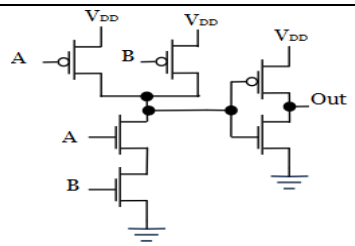

Figure 4. XOR implementation using CMOS

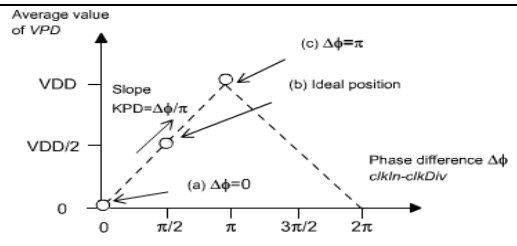

Figure 5. The XOR Phase Detector

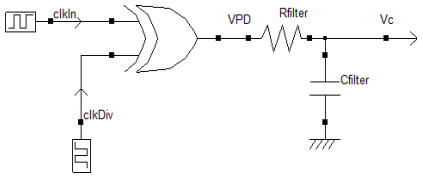

Figure 6. XOR gate with Filter

Table 1. Truth Table

Clk_in	Clk_div	XOR
0	0	0
0	1	1
1	0	1
1	1	0

The filter of DPLL is used to transform the instantaneous phase difference V_{PD} into an analog voltage V_C which is equivalent to the average voltage V_{PD}. The rapid variations of the phase detector output are converted into a slow varying signal V_C by filter, which will later control the voltage controlled oscillator. The filter is large capacitor C, charged and discharged through the R resistance. The RC delay creates a low-pass filter. Figure 6 shows an XOR gate with output charged with a capacitor and a serial resistance to create the desired analog voltage control V_c, [2, 6]. For RC low pass filter, when V_{PD} is input, output V_C is,

$$V_C = \frac{1}{RC}\int_0^T V_{PD}\,dt \qquad (4)$$

$$= \frac{1}{RC} \times V_{PD}(t)_0^T$$

$$= \frac{V_{PD}}{RC} \times T$$

$$V_C = \frac{V_{PD}}{RC} \cdot \frac{1}{f} \qquad (5)$$

R=1000 Ω , C=0.3pF, f =2.4GHz

$$V_C = \frac{0.45}{1000 \times 0.3 \times 10^{-12}} \cdot \frac{1}{2.4 \times 10^9}$$

$$V_C = 0.625V$$

As DPLL is locked when $V_c = V_{DD}/2$, thus providing a permanent current path through Rvdd2 to $V_{DD}/2$, which helps in keeping V_c around $V_{DD}/2$. Therefore, V_c taken as 0.44V, given as input to VCO.

The voltage controlled oscillator (VCO) generates a clock with a controllable frequency. The current-starved VCO is shown schematically in figure 7. As frequency of oscillations depends on delay introduced by each inverter stage so delay should be voltage controlled. One way to control the delay is to control the amount of current available to charge or discharge the capacitive load of each stage. This type of circuit is called a current starved ring VCO. In this VCO basically the control voltage (V_c) modulates the turn-on resistances of the pull-down transistor and pull-up transistors through a current mirror. These variable resistances control the

current available to charge or discharge the load capacitances. Large value of V_c allows a large current to flow, producing a small resistance resulting into small delay. Current starved ring VCO uses variable bias currents to control its oscillation frequency.

Its operation is similar to the ring oscillator. The current-starved inverter chain uses a voltage control V_C to modify the current that flows in the M5, M6 branch. MOSFETs M2 and M3 operate as an inverter, while MOSFETs Ml and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for current. The drain currents of MOSFETs M5 and M6 are the same and are set by the input control voltage V_C. The currents in M5 and M6 are mirrored in each inverter/current source stage, [2, 4].

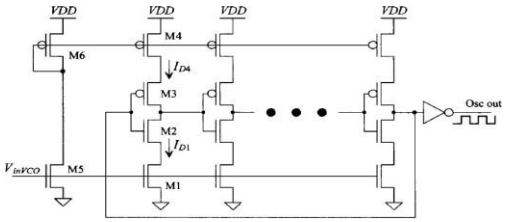

Figure 7. Current Starved VCO

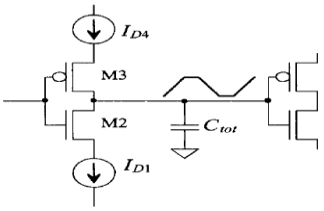

Figure 8.Simplified view of a single stage of the current-starved VCO

Figure 8 shows the simplified view of a single stage of the current-starved VCO. The time taken to charge C_{total} from zero to V_{SP} with the constant-current I_{D4} is given by

$$t_1 = C_{total} \cdot \frac{V_{SP}}{I_{D4}} \quad (6)$$

While the time it takes to discharge C_{total} from V_{DD} to V_{sp} is given by

$$t_2 = C_{total} \cdot \frac{V_{DD} - V_{SP}}{I_{D1}} \quad (7)$$

If we set $I_{D4} = I_{D1} = I_D$ (which we will label $I_{Dcenter}$ when $V_{inVC0} = V_{DD}/2$), then the sum of t_1 and t_2 is simply

$$t_1 + t_2 = C_{total} \cdot \frac{V_{DD}}{I_D} \quad (8)$$

The oscillation frequency of the current-starved VCO for N (an odd number > 5) of stages is

$$f_{osc} = \frac{1}{N\,(t_1 + t_2)} = \frac{I_D}{N.C_{total}.V_{DD}} \quad (9)$$

Which is equal to f_{center}*(@*$V_C = V_{DD}/2$ and $I_D = I_{Dcenter}$*)*

Where,

$$I_D = W.C'_{OX}.v_{SAT}.(V_{GS} - V_{THN} - V_{DS,SAT}) \quad (10)$$

$$C_{total} = C'_{OX}.(Area).(Scale)^2 \quad (11)$$

Table 2. MOSFET Parameter

MOSFET parameters for scale factor of 45 nm		
Parameter	NMOS	PMOS
$V_{DS,SAT}$ and $V_{SD,SAT}$	0.045V	0.045V
V_{GS} and V_{SG}	0.44V	0.44V
VTHN and VTHP	0.28V	0.28V
vsatn and vsatp	$110 * 10^3$ *m/s*	$90 * 10^3\, m/s$
Tox	$14\,A^0$	$14\,A^0$

For the Ratio of W/L,

$$(W/L)_p = 2.5(W/L)_n \quad (12)$$

Also the values of L for NMOS and PMOS are same in 45 nm technology, therefore

$$L_p = L_n = 45nm$$

So, the ratio will be

$$W_p = 2.5Wn$$

By putting the values of W_n=180nm in above equation, we get

$$W_p = 450nm$$

Finally the ratio of W/L for NMOS & PMOS in 45nm technology:

For NMOS: $W_n = 180nm$, $L_n = 45nm$.

For PMOS: $W_p = 450nm$, $L_p = 45nm$

By putting the values of these parameters in the equation of I_D, therefore

$$I_D = 180\times10^{-9} \times 25\times10^{-3} \times 110\times10^{3} \times (0.44 - 0.28 - 0.045)$$
$$I_D = 56.92\times10^{-6}\,A$$

$$C_{total} = 25\times10^{-3} \times \frac{5}{2}(10\cdot1 + 4.1).(45\times10^{-9})^2$$
$$C_{total} = 1.77\times10^{-15}\,F$$

$$f_{osc} = \frac{\Delta I_D}{N.C_{total}.V_{DD}}$$

$$f_{osc} = \frac{56.92 \times 10^{-6}}{5 \times 1.77 \times 10^{-15} \times 0.9}$$

$$f_{osc} = 7.14 \times 10^{9} Hz$$

IV. IMLEMENTATION

The trend of CMOS technology improvement continues to be driven by the need to integrate more functions into given area of silicon. Table 3 gives an overview of the key parameters for technological nodes from 180 nm, introduced in 1999 to 11 nm in 2015. For thinner the gate oxide, transistor current is high and thus high switching speed. The SiO_2 has been regularly scaled down, but has reached a physical limit of five atoms with the 90 nm CMOS process. With the 45 nm technology, new materials such as metal gates together with high-permittivity oxide are introduced, [3, 5]

Table 3. Technological Evolution and forecast

Technology node	**180nm**	**130nm**	**90nm**	**65nm**	**45nm**	**32nm**	**22nm**	**16nm**	**11nm**
First Production	1999	2001	2003	2005	2007	2009	2011	2013	2015
Gate Length	130nm	70nm	50nm	35nm	30nm	25nm	18nm	12nm	9nm
Gate material	Poly SiO_2	Poly SiO_2	Poly SiO_2	Poly SiO_2	Metal High K	Metal High K	Metal High K	Metal High K	Metal High K
Memory point u^2	4.5	2.4	1.3	0.6	0.3	0.17	0.10	0.06	0.006

A smaller feature size means smaller transistors can be carved onto silicon. Smaller transistors require less voltage to operate and therefore, use less power. A nanometer is a billionth of a meter. Its ten angstroms.

The complete DPLL using 45 nm VLSI technology is shown in figure 9. This circuit is implemented with 16 NMOS transistor and 15 PMOS BSIM4 transistors with optimum dimensions of transistors and metal connections according to the Lambda based rules of microwind 3.1 software. This implementation includes a filter register of 1000.0Ω. The virtual capacitor C_{filter} is fixed to 0.3pf. This resistance and capacitance are easy to integrate on-chip. During the initialization phase, the precharge is active & control voltage Vc rapidly change to $V_{DD}/2$. Then, the VCO outputs starts to converge to the reference clock. Then Vc tends to oscillate and stable where the PLL is locked and stable. To obtain the layout of proposed PLL, CMOS circuit of each element of proposed PLL is converted into physical layout using lambda based rules of microwind 3.1 software. After cascading the layout of each element, final layout is obtained. [5,6].

Table 4. Key Features of 45 nm Technology

Sr. No.	**Parameter**	**Value**
1	VDD (V).	0.40 -1.2 V
2	Ioff N (nA/μm)	5-100(nA/μm)
3	Ioff P (nA/μm)	5-100 (nA/μm)
4	Gate dielectric	SiON, HfO2
5	No. of metal layers	6-8

Compared to 65-nm technology, 45 nm technologies is preferably used because

1. 30% increases in switching performance
2. 30 % reduction in Power consumption
3. 2 times higher density
4. 2 times reduction of the leakage between source and drain and through the gate oxide.

Considering the advantage of 45 nm technologies over 90 nm & 65 nm technologies, the proposed work is implemented using 45 nm technologies.

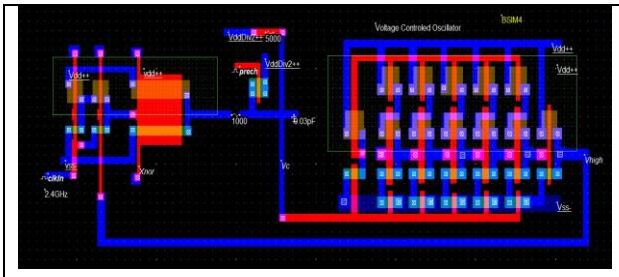

Figure 9. Layout of Phase locked loop using 45nm VLSI technology.

The Software Microwind 3.1 used, allows designing and simulating an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. It also includes all the commands for a mask editor as well as original tools such as 2D and 3D process view, Verilog compiler, tutorial on MOS devices. It is easy to access the Circuit Simulation by pressing one single key. The electric extraction of circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

V. RESULT

In this section, DPLL is designed and results of each component of DPLL are mentioned. The input output voltage versus time waveforms of DPLL are shown in figure 10 and figure 11. Also simulation results of the circuit in terms of frequency versus time are shown.

Phase Detector

The phase detector of the DPLL is used here is XOR gate. When locked, the phase difference should be close to π /2 and V_{PD} is V_{DD}/2.Thus, for V_{DD}=0.9 V, the phase detector is locked at 0.45 V. Figure 10 and 11 shows simulation of DPLL of figure 9, which shows Voltage versus time response for input frequency of 2.4 GHz.

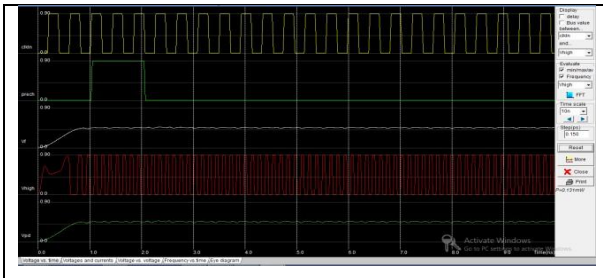

Figure 10. Simulation of DPLL of figure 9 (Voltage versus time)

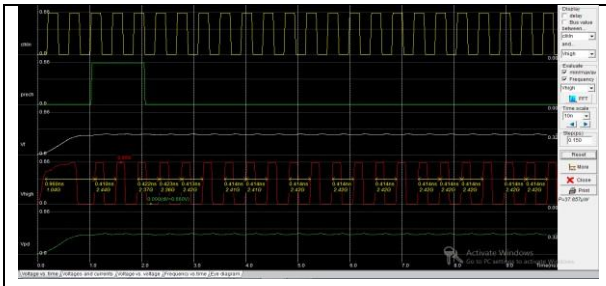

Figure 11. Simulation of DPLL of figure 9(Voltage versus time)

Loop Filter

It is the loop filter that determines the dynamic characteristics of the DPLL. The filtered signal controls the VCO. The filter is large capacitor C, charged and discharged through the Ron resistance. The R_{on}.C delay creates a low pass filter.

VCO

A Voltage-Controlled Oscillator (VCO) is a circuit that provides a varying output signal (typically of square-wave or triangular-wave) whose frequency can be adjusted over a range controlled by a dc voltage. A voltage controlled oscillator or VCO is an electronic oscillator whose oscillation frequency is controlled by a voltage input. The applied input voltage determines the instantaneous oscillation frequency. Figure 11 shows voltage verses time waveforms of DPLL's input and outputs. The current starved oscillator is used as a VCO for the DPLL. The DPLL shown in figure 12 is locked at 7.1 GHz frequency when control voltage reaches to 0.9V. For the input frequency of 2.4 GHz, DPLL shows different output frequencies as shown in table 5. When control voltage is reaches to 0.66 volt, DPLL is locked to the frequency of 2.4 GHz.

Table 5. V_{DD} with respect to Output Frequency

Input frequency of 2.4 GHz	
V_{DD}	Output Frequency
0.9 V	7 GHz
0.66V	2.4GHz

Table 6. Power dissipation with respect to V_{DD}

V_{DD}	**Power Dissipation**
0.9V	0.131m W
0.66V	37.857uW

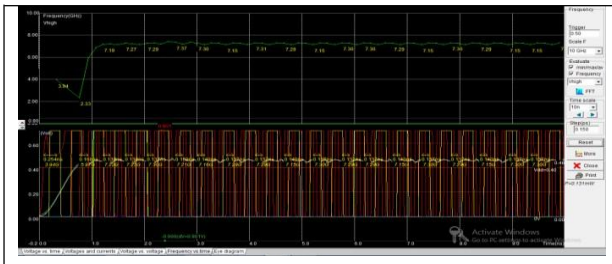

Figure 12. Simulation of DPLL of figure 9 (Frequency versus time)

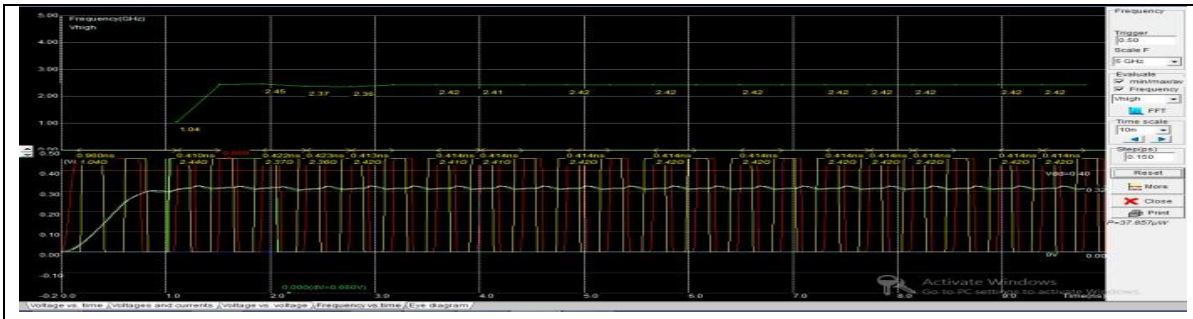

Figure 13. Simulation of DPLL of figure 9(Frequency versus time)

Change in power verses V_{DD} is shown in following table 6. It is found that with the supply of 0.9 volt, the total power consumption of the PLL circuit is 0.131 miliwatt. And when VDD decreases power dissipation also decreases to 37.857 microwatt. Figure 14 shows input-output frequency relation.

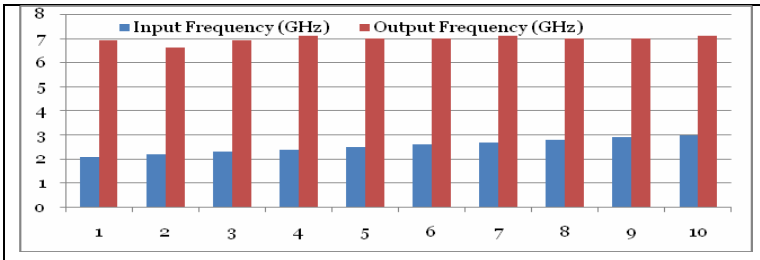

Figure 14. Input-Output Frequency relation

VI. CONCLUSION

In this paper, we proposed to design DPLL using 45 nm CMOS technology and implemented using microwind 3.1. For an input frequency of 2.4 GHz, two different frequencies are generated as 7GH and 2.4GHz. The comparison was done after simulation of its schematic. Also it is observed that at different input frequencies the output frequency is remains constant as shown in figure 14. For change in input frequency 2 GHz to 3 GHz the output frequency remain constant at 7Ghz. It known that the DPLL generated frequency of 2.4GHz is used for ZIGBEE applications which are also useful for 4G communication with frequency range of 1.8GHz-3GHz. It is also observed that as V_{DD} increases its power consumption of the circuit is also increased and vice versa. The lock range for the DPLL is 832 MHz and lock time is 1.57 n sec was observed as expected.

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