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An Improved Voltage follower Canonical Switching Cell Converter with PFC for VSI Fed BLDC Motor

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Abstract : *This paper describes a power factor improvement of canonical switching converter for BLDC motor by using voltage follower technique. In this paper (BLCSC) Bridge Less Canonical Switching Cell Converter runs in a discontinuous inductor current mode. Due to this near unity power factor is obtained. The DC link voltage at the front end of VSI fed BLDC motor is changed to control the speed of the motor with the help of PFC converter. From the above action, VSI which works in a fundamental frequency switching when it is electronically commutated minimizes the switching losses. Conduction losses are also reduced by eliminating the DBR circuit in CSC configuration in the existing system. The proposed arrangement provides a considerable improvement in the performance when the result is being matched up with the existing system. Execution of proposed drive is certified by the observed results from the modified model simulated using PROTEUS.*

Keywords*- Inverter - VSI – Voltage source Inverter, BLDC – Brush Less DC motor, BLCSC –Bridge Less Canonical Switching Cell converter, PFC-Power Factor Correction, DBR-Diode Bridge Rectifier, Power quality.*

I. INTRODUCTION

BLDC- motors have acquired importance in the recent ten years due to development in quality of power that framed an unmatched performance when compared to existing drives [1]. Some of the reasons made this motor more famous in industries. That reason is as follows: high reliability, high performance, high ruggedness, reduced electromagnetic interference problems, and exceptional performance over an extensive range of speed control [2,3].This machine is more applicable for many low power and medium power applications such as position actuators, ventilation, household appliances, air conditioning and heating, medical equipment. Hall sensors are used to remove the tribulations related to the existing DC motors. The problems removed from the sensor are EMI, sparking noise, maintenance problem, etc. The higher value of the DC link capacitor fed VSI based BLDC motor follows the diode bridge rectifier to drag large current from supply and insert a large value of lower order harmonics in the circuit. As an effect of this operation the power factor value is poorly (even lower than 0.75) and large THD of current (even as more as 60%) at the supply mains. For this reason, quality of power of AC mains was improved by using power factor correction converters. In the collection many forms of one – stage power translation techniques with isolation or in the absence of isolation were sighted. These converter [6] circuits have a smaller amount of devices and therefore have small losses linked with them. The expenditure of these converter design becomes an imperative parameter based on the quantity of sensing constraint and the type of process of the PFC converter. The choice of working mode is a transaction between the price and tolerable stress on the switch because a current multiplier technique can be used when the circuit works in uninterrupted conduction operating mode which results in less stress on the switch but it required more than a sensor whereas one potential sensor is required for the PFC converter switch. So that the option of interchange working mode will be an exchange between the price and the allowable pressure on switch. A CSC -converter fed Brushless DC motor with PFC configurations has been narrated in the review. [1] Proposed a conventional PFC converter to fed Brushless DC motor system. The fixed DC voltage from the Link capacitor and PWM control of BLDC motor is used. It is found that the whole system is severely affected because of the heavy switching stress. Also Cheng suggested a three phase VSI fed BLDC motor drive, with an active rectifier required a difficult control. Switching losses of VSI are greatly minimized by changing the DC voltage out of the converter. In general BLDC motor electronic commutation requires low frequency switching VSI, the circuit uses the same principle to decrease the switching losses. A variable voltage control is fed by the (SEPIC) single-ended primary-inductor converter in the front end of the BLDC motor. .This paper explains about the improvement of a reduced sensor based BLDC motor drive for low power applications. In the last ten years, Due to the low conduction losses it has more profit at the front end. The bridge less buck and boost converter is used for limited voltage conversion so it could not support wide range of control voltage. Likewise many components are used with a high order PFC bridge. The advantage of using a canonical switching cell converter are better performance, pre regulator power factor, good light load condition and small component count. Fig.1. Shows Traditional PF Correction embedded on a CSC converter. Canonical switching cell converter circuit contains the combinations of switch (SW), diode (D), capacitor (C_1). This cell combines with the inductor (L_i) and DC link capacitor (C_d). This is known as a Canonical switching cell converter. By making the circuit in a proper way that is with selected parameters PFC correction will be achieved when the circuit is fed with an arrangement of AC Supply, Diode Rectifier and Filter. The aim of this paper is to offer a reduced conduction loss by removing the DBR and also used to offer an economic solution to the discussed problems.

The figure1 Shows the conventional PFC based CSC Converter which has a Diode Bride Rectifier (DBR) which will introduce Harmonics in the system.

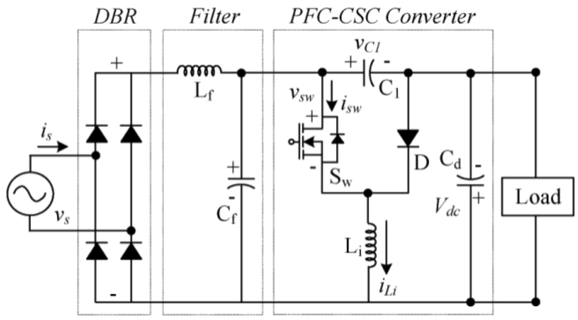


Fig 1 Conventional PFC based CSC converter

II. PFC BASED BRIDGE LESS -CSC CONVERTER FED BLDC MOTOR

Fig. 2 explains about BLCSC converter for VSI-fed brush less DC motor drive. Here converter diode bridge rectifier is neglected. So that conduction loss gets reduced. This converter works in (DICM) dis-continuous inductor current operating mode. Inductor currents (Li1, Li2) are broken. Although voltage across intermediary capacitors (C1, C2) are continuous in a switching period. A changeable DC link voltage is used to control the speed of the BLDC motor are shown below. Switching losses are decreased in VSI, when it is electronically commutated. The execution of projected drive is compared with the experimental results received from a planned model with better quality of power from supply for a vast range of speed. Owing to this better voltage exchange ratio, it is used for controlling speed of BLDC motor over a wide range. When compared to other BL configurations of SEPIC, CUK [8] AND ZETA converters, and BLCSC converters have less components and less number of power electronic devices at every half cycle. When supply voltage is given. The proposed model shows fewer amounts of conduction losses owing to the usage of conducting devices at half cycle.

- The following Table I justifies the selection of Bridgeless CSC. The physical characteristics of BLCSC are compared with other available topologies and the result has been tabulated. It shows that it uses only less components per half cycle of operation. This will automatically reduce the stress on the components. The losses also get reduced with reduction in the number of components under conduction for every half cycle. Though the total number of components used is same as that of BL-Buck Boost, the number of components under conduction is comparatively less.

TABLE I COMPARISON OF PROJECTED BRIDGE LESS CSC CONVERTER WITH OTHER RELEVANT STRUCTURES.

Configuration	No of Devices					1/2 Period
	Sw	D	L	C	Tot	
BL-Buck Boost [7]	3	4	1	3	11	8
BL-Cuk[8]	2	4	4	3	13	7
BL-Sepic	2	3	2	2	9	7
BL-Zeta	2	4	4	3	13	7
Proposed BL-CSC	2	4	2	3	11	6

III. WORKING OF THE PFC BASED BRIDGE LESS - CSC CONVERTER

The working of the BL-CSC converter is divided into two key categories.

A. *Working in Positive half cycle and negative half cycle of Input AC Supply*

When supply voltage is applied to the bridge less converter, for each positive and negative half cycles one switch will conduct. Fig. 3a–f explains about the working of the projected model for each positive and negative half cycles. Input current flows through diode D_p, inductor Li, and switch Sw1 during the positive half cycle as shown in 3a-c.Equivalently switch Sw2, diode D_n and inductor Li2 are operating in a negative half cycle as shown in the figure 3d-f.Fig. 4a explains about the waveforms of input AC voltage with inductor current (iLi1 and iLi2) and midway capacitor voltages (VC1 and VC2). The projected model is working in discontinuous inductor current mode. *Due* to this inductor currents are discontinuous and voltage across the capacitor is continued during the switching period.

B. *Operation during Complete Switching Period*

The proposed brush less canonical switching cell converter is constructed to work in DICM. Figure 3(a-f) tells about the working of different modes of operation for every half cycle of the input AC voltage,

MODE 1 (A): During the first mode(A) switch Sw1 is in ON condition, inductor Li1 begins charging in the input side through the diode D_p and current iL1 increases, whereas intermediate capacitor C1 begins discharging through switch Sw_1 to charge C_d. For this operation V_{c1} decrease and V_{dc} increase.

MODE I (B): During mode B switch Sw1 is in OFF condition. If Sw1 is OFF then inductor Li1 discharges to DC link capacitor through diode D1 (Figure 3b). Owing to this the current i_{L1} decreased. The voltage across the DC link increases continuously during this mode of operation. The capacitor C1 starts charging, which increases the voltage V_{c1}.[11]

MODE I-C: During the discontinuous mode of operation the current which flows all the way through the inductor Li1, becomes zero (Figure 3c). The capacitor C_d delivers the necessary demand of the load. At the same time capacitor C_1 holds the energy continues to retain its energy. The equivalent operation of the converter is observed for negative half cycle of input, whereas inductor (L_{i2}), capacitor (C_2) and diodes (D_1 and D_2) conducts in the same way (Figure 3d-f).

The most concentrated Mode of operation is the Discontinuous mode of working in which both the inductors gets completely discharged thus their current becomes zero, also both the capacitors starts charging refer figure 3c and 3f for positive and negative half cycles. These modes results in improved power factor since inductor current become zero for a particular interval of time.[14]

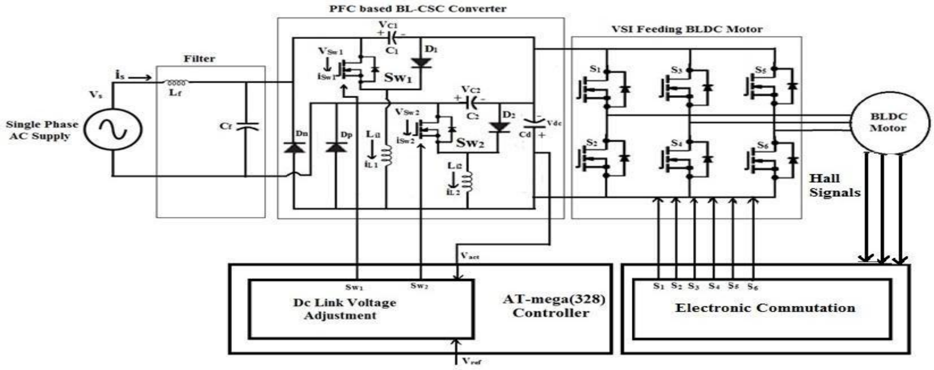


Fig 2 Projected PFC based Bridge Less- CSC converter feeding BLDC motor system

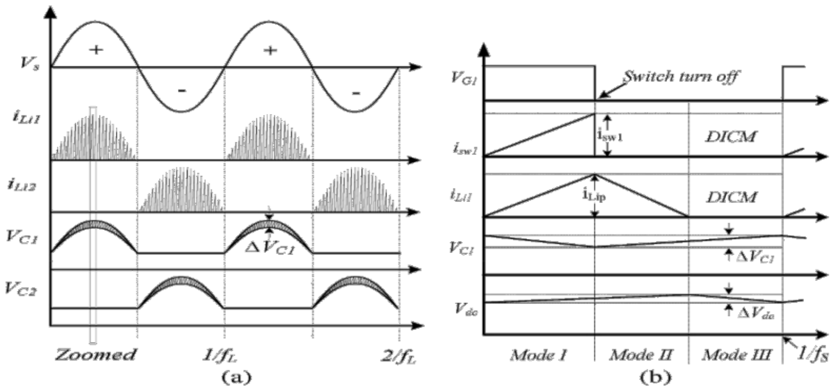


Fig 3 Waveforms for various states of working for Proposed BL-CSC Converter

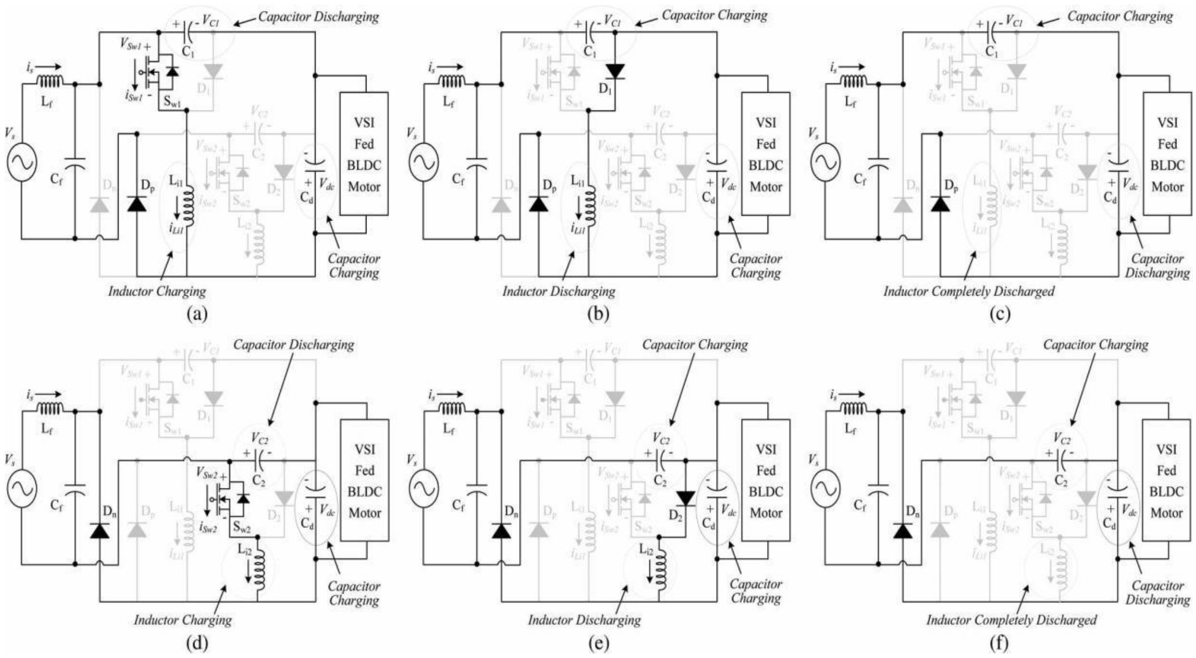


Fig 4 Various modes of working on the projected Bridgeless - CSC converter. (a) (b) and (c) : Mode I (A), (B) and (C) respectively, (d) and (e) : Mode II(A) and (B) respectively, (f): Mode II (C)

IV. DESIGN PROCEDURE FOR PFC BASED BRIDGELESS - CSC CONVERTER

The projected PFC converter [5] is modeled to work with Discontinuous ICM . So that, the inductor current iLi1 and iLi2are discontinuous and the capacitor C1 and C2 voltage are continuous during switching operation. For experimental studies 424-W BLDC motor is used the input side converter of 500W (Pmax) is considered to supply a BLDC motor drive .The speed can be varied widely from low value corresponding to 70V (Vdc min) value to the maximum voltage of 320 V(Vdc max) by using DC link voltage control.[12]

The input voltage can be given by,[15]

$V_s(t)=V_m \mathrm{Sin}(\omega t)=220(\sqrt{2}) \times \mathrm{Sin}\,(314t)$ (1)

Where $V_m \rightarrow$ maximum input voltage, (ie.,$\sqrt{2}\, V_s$)

The value of voltage which appears across the inductor combination and any of the switches are given as $V_{in}(t) = \left| V_m \sin(2\pi f t) \right| = \left| 220(\sqrt{2}) \times \sin(314t) \right|$ (2)

The voltage output V_{dc} of the CSC converter is given as follows,

$$V_{DC} = \frac{\alpha}{1-\alpha} V_{in} \quad (3)$$

$\alpha \rightarrow$Duty ratio

The value of α(t) based on voltage input $V_{in}(t)$ and the desired voltage the DC link V_{DC}. The instantaneous duty cycleα(t) is acquired by substituting equations 2 and 3 as follows,

$$\alpha(t) = \frac{V_{dc}}{V(t)+V_{dc}} = \frac{V_{dc}}{|V_m \sin(\omega t)| + V_{dc}} \quad (4)$$

If the voltage across the DC link is changed, then the speed of the drive will be varied, therefore the P_i is noted a linear utility of V_{dc} as

$$P_i = \frac{P_{max}}{V_{dcmax}}(V_{dc}) \quad (5)$$

Where V_{dc} is the DC link voltage .

P_{max} - Desired power for the PFC converter

P_{max} represents the maximum power that can be transferred by the proposed Bridge less Canonical Switching cell converter.

A. DESIGN OF INPUT INDUCTORS (LI1 AND LI2) IN DISCONTINUOUS CURRENT CONDUCTION:

The significant value of input inductor L_{ic} is as follows

$$L_{ic} = \frac{Vin(t)\, D(t)}{2 I_{in}(t) f_s} = \frac{Rin\, D(t)}{2 f_s} = \left(\frac{V_s^2}{2 f_s}\right) \quad (6)$$

$R_{in} \rightarrow$ input resistance

$f_s \rightarrow$ switching frequency and

$P_i \rightarrow$ instantaneous power.

The value of $L_{ic\ min}$ is calculated as

$$L_{ic\ min} = \frac{V_{smin}^2}{P_{max}} * \frac{D(t)}{2 f_s} = \frac{85^2}{500} = \frac{0.7206}{2*20000} \approx 260\ \mathrm{Mh} \quad (7)$$

To attain the discontinuous current transmission by picking the minimum requirement of input inductors (L_{i1} and L_{i2}) which should be less than $L_{ic\ min}$ (35).Hence the values of $L_{i1}=L_{i2}$=70 µH to accomplish intermittent current transmission The manifestation for C_1 and C_2 are,[10]

$$C1 = C2 = \frac{V_{dc} D_t}{\Delta V_{in}(t) f_s R_L} = \frac{V_{dc} D_t}{\eta\{V_{in}(t)+V_{dc}\} f_s R_L} \quad (8)$$

V_{dc}= legalized ripple voltage athwart in-between capacitors C1 and C2

Vc = middle capacitor voltage

R_L = rivaled load resistance

$$R_L = \frac{V_{dc}^2}{P_i}$$

$$C1=C2 = \frac{V_{dcmax} D(t)}{\eta\{\sqrt{2} V_{smax}(t) + V_{dc}\} f_s R_L}$$

$$= \frac{320 * 0.4481}{0.1\{270\sqrt{2}+310\}\, 20000 * 192.2} = 0.522\mu F \quad (9)$$

B. STRATEGY OF DC LINK CAPACITORS (CD):

The value of Cd is as follows

$$Cd = \frac{I_{dc}}{2\omega \Delta V_{dc}} = \left(\frac{P_i}{V_{dc}}\right) \frac{1}{2\omega\kappa V_{dc}} \quad (10)$$

If the value of DC link voltage is minimum then the design will in the worst case. It is expressed as Cd,

$$Cd = \left(\frac{P_{min}}{V_{dcmin}}\right) \frac{1}{2\omega \Delta V_{dcmin}} = \left(\frac{113}{70}\right) \frac{1}{2*314*0.02*70}$$

$$= 1836\mu F \quad (11)$$

Hence we can choose a electrolytic capacitor of 2200 μF. In general, the selection of capacitance should be given more importance in designing any converter circuit.

A. Strategy Of Filter Parameters (Lf And Cf):

The top order harmonics in the supply system are decked with the help of low pass LC filters. The extreme rate of filter capacitance is given as,

$$C_{max}=\left(\frac{I_m}{\omega_L V_m}\right)\tan(\theta) = \left(\frac{P_o\sqrt{2}V_s}{\omega_L V_m}\right)\tan(\theta)$$

$$= \frac{\left(\frac{500\sqrt{2}}{220}\right)}{314 * 220 * \sqrt{2}V}\tan(0.99^{\circ}) = 564.27 \text{ nF} \qquad (12)$$

Therefore, C_F of 330 NF is selected.

The auxiliary value of inductance obligatory is given as

$$L_f = L_{req} + L_s = \frac{1}{4\pi^2 f_c^2 C_f} = Lreq + 0.05\left(\frac{1}{\omega_L}\right)\left(\frac{V_s^2}{P_o}\right)$$

$$L_{req} = \frac{1}{4\pi^2 * (2000^2) * 330 * 10^{-9}} - 0.05\left(\frac{1}{314}\right)\left(\frac{220^2}{500}\right)$$

$$= 3.75\text{mH} \qquad (13)$$

Therefore f_c can reserved approximately to fs /10.

This LC filter taking inductance Lf (3.77mH) and capacitance CF (330 nF). We can choose a film capacitor with a polypropylene dielectric for nourishing the high frequency current ripple reduction in the existing converter.

The Design of this L_f and L_{req} is very important for any type of Converter. Any error in the design will result in vast changes in the expected result like harmonics, poor power factor etc., which are not acceptable.[21]

V. CONTROL OF PROPOSED CONVERTER FED BLDC MOTOR SYSTEM

In our motor drive voltage supporter system is used. A single potential sensor is desirable for monitoring the converter output .So that the rotation of motor is meticulous .

The error voltage is specified as[17]

$$V_e(\kappa) = V_{dc}(\kappa)^* - V_{dc}(\kappa) \qquad (14)$$

A. CONTROL OF BLDC MOTOR:

The electronic commutation of BLDC motor is found by identifying the rotor position with the help of hall effect position sensor. Rotor position material is used to turn ON and OFF the switches in VSI to follow the current flow in separate windings.[24]

Rotor position can be detected on a span of 60˚ by spending hall effect position sensor (H_a, H_b, H_c).[18]

Fig 5 shows conduction states of 2 switches S_1 and S_4. The line current (I_{ab}) is obtained from DC link ,whose magnitude based on the functional DC link voltage V_{dc},the back emf e_{an} and e_{bn} , resistance(R_a & R_b),mutual inductance and self inductance (M,L_a,L_b) of the stator windings. The altered switching states of the VSI feeding a BLDC motor based on the Hall Effect position signal (H_a-H_c) which is expressed in table II.[19]

TABLE II HALL SIGNALS AND THE SWITCHING STATES OF VSI

Degree	Hall Signals			Switching States					
	H	H	H_c	S_1	S_2	S_3	S_4	S_5	S_6
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-	0	1	1	0	0	1	0	0	1
180-	1	0	0	0	0	0	1	1	0
240-	1	0	1	1	0	0	1	0	0
300-	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

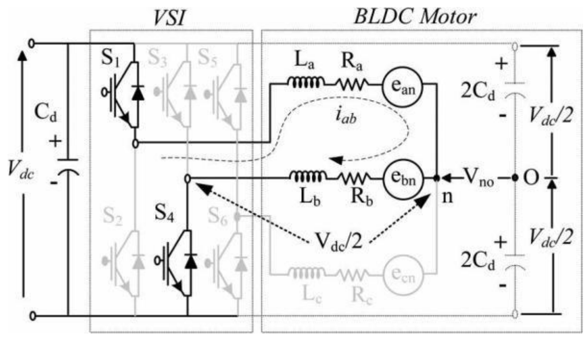


Fig 2 Conduction of a 3ϕ VSI feeding BLDC motor

VI. OUTCOMES AND DISCUSSION

The performance of the projected concept was established as a hardware prototype which was experimentally confirmed. In our scheme Atmega328 Controller is used to grow our drive. In between the Controller and the gate driven of the VSI the Opto separation is decided. 6N136 Opto couplers are used in PFC switches. Hall Effect position sensors, hall signal filtering and power circuitries are also established. The acceptable procedure of BLDC motor is done by detecting of rotor position with the help of Hall sensors. The DC link voltage of the BLCSC is adjusted to control the rpm of BLDC motor. Now we are going to see about the test results of our paper. They are as follows

A. PERFORMANCE OF THE PFC BL-CSC CONVERTER AS POWER FACTOR PRE-REGULATOR

The BL-CSC converter is shown to work in DICM .So that the current flows through the inductor L_{i1} and L_{i2}, These values are fit for a PFC converter of rating 0.5KW operating in Discontinuous ICM. Owing to this procedure in high current stress is detected at the PFC converter[13].

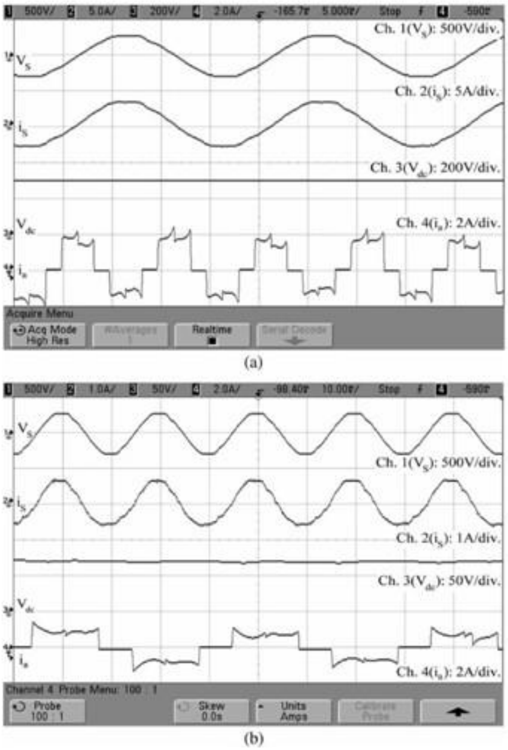
B. PFC and Improved Power Quality at AC mains

This content compacts with practical quality of power guides at the supply mains to operate our BLDC drive.

a) Three different types of waveforms are found during power quality guides. They are as follows: i) In this wave from 4 different cases are exhibited about i) RMS value ii) frequency iii) crest factor (CF) of supply voltage and supply current.

b) In this set of waveform active, reactive and apparent power as well as power factor(cosϕ) and the displacement power factor at AC mains.[16]

c) In this third set harmonic spectrum and the obtained THD of supply current at AC mains.



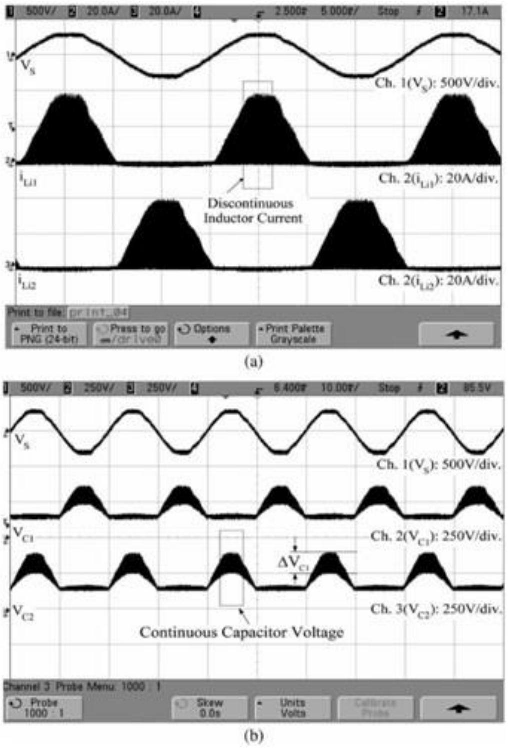


Fig 6 Developed drive performance at different voltage levels Fig 7Inductor current and capacitor voltage waveform at different voltage and speed ranges

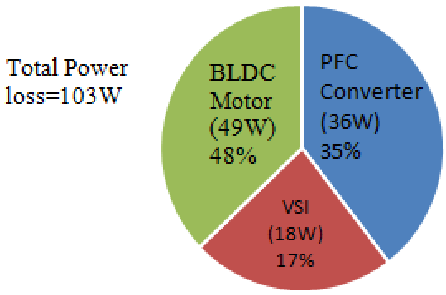


Fig 8Percentage of losses in different parts of the proposed BLDC motor drive

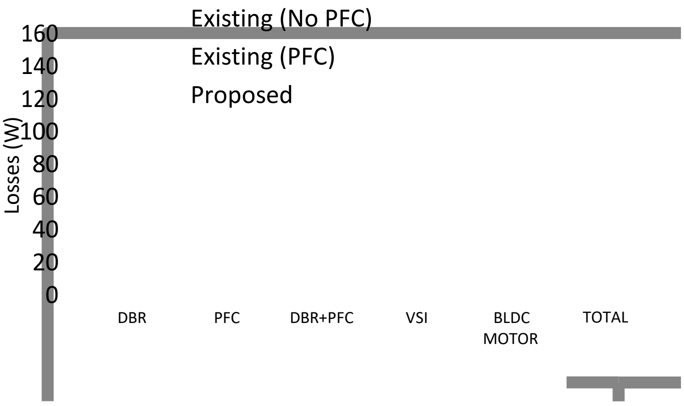


Fig 9 Comparative analysis of losses of the proposed drive with the conventional scheme.

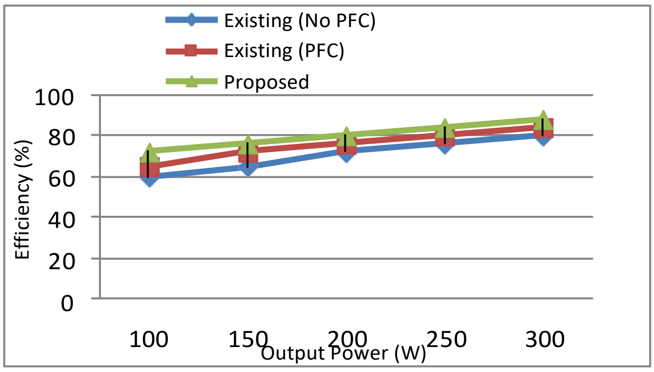


Fig 10 Comparative analysis of efficiency of the proposed drive with the conventional scheme.

TABLE III COMPARISON OF EXISTING DBR-CSC AND PROPOSED BL-CSC

Existing DBR -CSC fed BLDC Motor	Proposed BL-CSC fed BLDC Motor
BLDC has very high losses.	Losses are low compared to BL-CSC fed motor DBR
It causes more switching losses so in this motor switching frequency are high.	Switching losses in VSI are significantly reduced ,because DBR at the front end converter is eliminated.
It has less efficiency. Fig 12 a&b	It has more efficiency. The efficiency increases in the order of 4% to 5%
BLDC has very high losses.	Losses are low compared to BL-CSC fed motor DBR
It causes more switching losses so in this motor switching frequency are high.	Switching losses in VSI are significantly reduced ,because DBR at the front end converter is eliminated.
It has less efficiency. Fig 12 a&b[23]	It has more efficiency. The efficiency increases in the order of 4% to 5%

VII. CONCLUSION

A power factor improvement of canonical switching converter for VSI fed BLDC motor using a voltage follower technique. It is used to increase the power quality of the AC mains .The DC link voltage at the front end of VSI fed BLDC motor is changed to control the speed of the motor with the help of PFC converter. From the above action, VSI which works in a fundamental frequency switching when it is electronically commutated, minimizes the switching losses. Conduction losses are also reduced by eliminating the DBR circuit in CSC configuration in the existing system. The quality of power is better at the supply mains to an substantial choice of speed and supply voltage in concern. Finally the desired output was obtained for the proposed drive. This is mainly suggested for low power applications.

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