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A Novel Reduced Switch Multilevel Inverter Using FPGA

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Abstract : *Multilevel inverters (MLI) are mostly used medium-voltage and high-power applications due to its attractive features. As the number of output voltage levels increases, the quality of the output voltage is improved leading to reduction of the filtering requirements. But multilevel inverter requires more number of power semiconductor switches as number of levels increase that increases cost and complexity in control circuit. In this paper, an innovative topology for multilevel inverter is proposed which reduces the number of switches considerably without increasing the total standing voltage of the switches. The proposed topology is a general topology which can be extended for any number of voltage levels. This topology as reduced switch multilevel inverter, we implement and generate the PWM by FPGA Spartron3E processor using VHDL language.*

Keywords - *Multilevel inverter (MLI), Field Programmable Gate Array (FPGA) & Driver.*

I. INTRODUCTION

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels[1]. The basic principle of the multilevel inverters is to divide the operating voltage of the inverter between power electronic switches so that low-voltage switches can be used to process high-voltage outputs. This capability has made the multilevel inverters suitable for high and medium voltage/power applications such as large motor drives, flexible AC transmission systems, VAR compensation and many other applications. On the other hand, increasing the number of inverter levels leads to achieving high-quality output voltages at low switching frequencies[2].

From topology point of view there are three well-established categories of multilevel inverters: neutral point clamped (NPC), cascaded H-bridge (CHB) and flying capacitor (FC) multilevel inverter[3]. The NPC inverter also known as diode-clamped multilevel inverter was the first topology of multilevel inverters. The three-level case of this topology was introduced in 1981. This inverter was based on a modification of the classical two-level inverter topology adding two new power semi-conductor devices. Following this topology, the FC multilevel inverter and CHB multilevel inverter have been presented. The above-mentioned multilevel inverter topologies have their own advantages and disadvantages. The common problem between them is that as the number of output voltage levels increases, the number of required power electronic switches increases considerably[4]. This results in high cost and complicated hardware circuit of the multilevel inverters. Therefore some researchers have made efforts to introduce new topologies of multilevel inverters with reduced number of switches. The conventional multilevel inverters can be used in hybrid form to get more advantages of multilevel inverters. Example of these hybrid multilevel inverters is series connection of the diode-clamped multilevel inverter and an H-bridge. Also combination of the FC and CHB topologies has been presented. This technique although improves the output voltage quality (by increasing number of levels) defeats the main aim of the multilevel inverters, that is, using low-voltage switches for high-voltage applications.

II. MATERIALS AND METHODS

A. System overview

The block diagram of the proposed multilevel inverter using FPGA is shown in figure 1. It has single phase rectifier, multilevel inverter and control circuit.

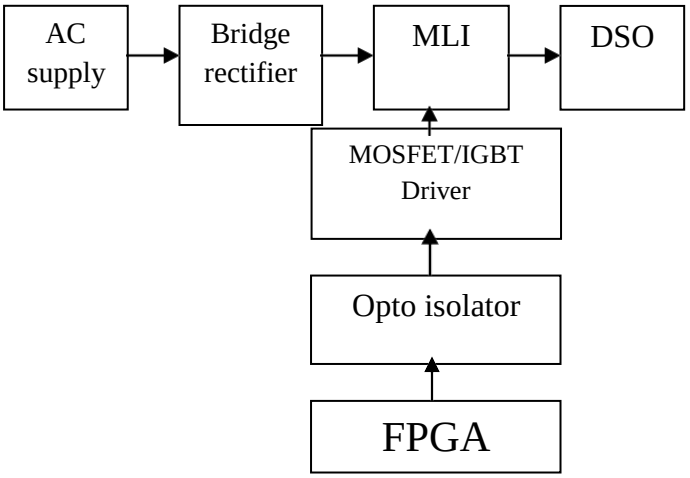

Fig. 1 Block diagram of proposed system**.**

In the proposed scheme the bridge rectifier is used to provide the dc voltage to the inverter circuit. The full bridge multilevel inverter has MOSFET switches. The inverter is followed by gate drive unit and a control unit. The primary function of the gate drive circuit is to convert logic level control signals into the appropriate voltage and current for efficient and reliable switching of the MOSFET module. In this paper an opto-coupler is used to isolate the gate drive circuit and the MOSFET based multilevel inverter circuit. [5]

B. Power circuit design

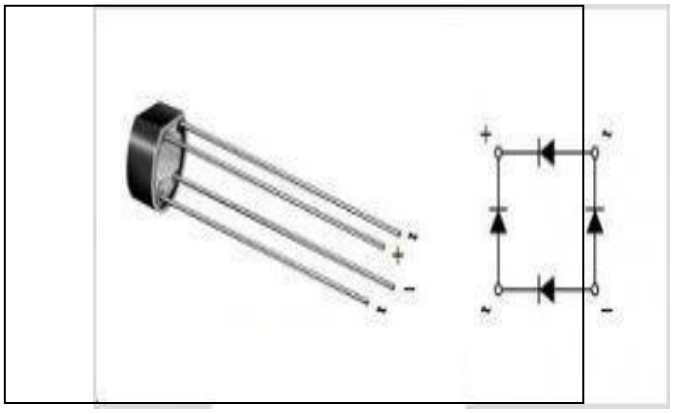

Fig.2 Bridge rectifier

The power circuit design contains full bridge rectifier, full bridge inverter assembly. Single phase 230V, 50 Hz AC supply is applied to the full bridge rectifier. This full bridge rectifier converts single phase AC input into DC. The DC supply is applied to the multilevel inverter which is made up of eight MOSFET switches.[6]

C. Control circuit

The control circuit of the proposed scheme consists of FPGA Spartan 3E processor. It is a semiconductor device containing programmable logic components called "logic blocks", and programmable interconnects.

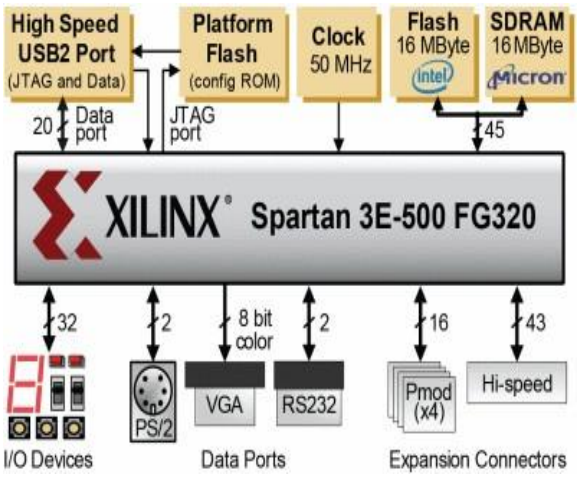

Fig.3 FPGA Spartan 3E Processor

The advantages of the FPGA are ability to re-program in the field to fix bugs, and lower non-recurring engineering costs. The proposed control system is designed by a FPGA based PWM inverter. VHDL language is used to develop the program. The device is programmed using XILINKX software. It is used to generate triggering pulse for MOSFETs.[7]

III. CIRCUIT DIAGRAM OF MLI

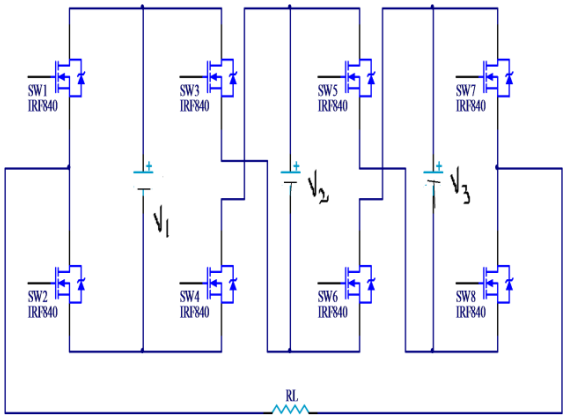

Fig.4 Reduced switch multilevel inverter using MOSFET

All eight MOSFET switches of the circuit are controlled by the PWM signals generated by the control circuit. The proposed system requires DC three voltage sources for the seven level inverter. In the complete experiment the Digital storage oscilloscope is used to observe the output waveform.[8]

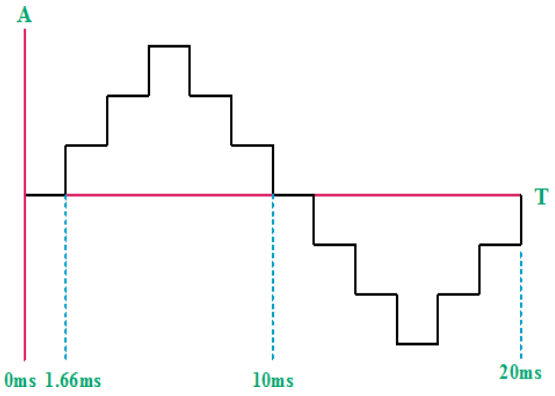

Fig. 5 Output seven level staircase waveform

IV. COMPARISON BETWEEN PROPOSED AND EXISTING MLI

The number of switches for the proposed topology has been calculated as NS= NL+ 1. For the CHB, the number of switches can be written as follows in terms of number of voltage levels NS,CHB= 2 (NL− 1). Here, NS refers the number of switches in the multilevel inverter circuit and NL refers the number of output voltage levels. It shows the number of switches for seven levels is 12 and for the same levels the proposed topology requires only 8 switches.[9] Hence, the proposed topology uses lower number of switches in comparison with the CHB topologies. Reduction in the number of switches at the same time reduces the number of required driver circuits for the switches and complexity of the inverter[10] and [11].

The other element of comparison is the number of devices in current path in any instant of time. This factor is important since it affects the total on-state voltage drop on the switches and also conduction losses of the switches. The number of the devices in current path (ND) can be considered as follows ND, proposed= (NL+ 1)/2,[13]-16] But in existing CHB topology, the number of devices can be calculated by using the equation ND, CHB= NL− 1.As the above equations show, the proposed topology has lowest series devices in current path which can lead to reduction in voltage drop and conduction losses of the switches. Here, ND stands for number of devices and NL stands for number of output levels.[17]

V. ADVANTAGES

The reduced switch multilevel inverter having the major advantages like Improving inverter reliability, Minimum harmonic distortion, Reduced number of switches, Low voltage switches also used and Decreases the complexity

As well as the cost of the circuit[18].

VI. CONCLUSION

For this proposed system, the MOSFETs of IRF840 types are used. Also the FPGA Spartan3E Processor is used to provide the gating signals for the switches. As the levels of output increases, nearly sinusoidal waveform will be obtained, this result in reduced THD. So the benefits of multilevel inverter include, lower transient power loss

Due to low-frequency switching, less THD, reduced ac filters, and possibility to replace MOSFETs with IGBTs, and thereby providing compact power conversion. It can be concluded that, in order to maintain the good quality of power, it is necessary to replace the conventional drives with 2 level inverters by multilevel inverters.

REFERENCES

[1] Veena B M , Triveni M T: „Hardware Implementation of 5 Level Inverter Using Microcontroller"

[2] Shivanand Masaraddi, Dr. M.S.Aspalli Ammar Masaoud: „Cascaded H-Bridge Multilevel Inverter Using PIC16F877A Controller"

[3] Babaei, E., Farhadi Kangarlu, M.: „Multilevel inverter with cross-connected st

[1] V. Bist and B. Singh, "An adjustable speed PFC bridgeless buck–boost converter-fed BLDC motor drive," IEEE Trans. Ind. Electron., vol. 61, no. 6, pp. 2665–2677, Jun. 2014.

[2] B. Singh and V. Bist, "An improved power quality bridgeless Cukconverter-fed BLDC motor drive for air conditioning system," IET PowerElectron., vol. 6, no. 5, pp. 902–913, May 2013.

[3] Ali, A. Nazar. "Performance Enhancement of Hybrid Wind/Photo Voltaic System Using Z Source Inverter with Cuk-sepic Fused Converter." Research Journal of Applied Sciences, Engineering and Technology 7.ISSN: 2040-7459; (2014): 3964-3970.

[4] Ali, A. Nazar X. "Ride through Strategy for a Three-Level Dual Z-Source Inverter Using TRIAC." Scientific Research publication 7.ISSN Online: 2153-1293 (2016): 3911-3921.

[5] Nazar Ali, A. "Performance Analysis of Switched Capacitor Multilevel DC/AC Inverter using Solar PV Cells." International Journal for Modern Trends in Science and Technology 3.05 (2017): 104-109.

[6] Ali, A.Nazar. "FPGA UTILISATION FOR HIGH LEVELPOWER CONSUMPTION DRIVES BASEDONTHREE PHASE SINUSOIDAL PWM -VVVF CONTROLLER." International Journal of Communications and Engineering 4.Issue: 02 (2012): 25-30.

[7] ali, A.Nazar. "A SINGLE PHASE HIGH EFFICIENT TRANSFORMERLESS INVERTER FOR PV GRID CONNECTED POWER SYSTEM USING ISPWM TECHNIQUE." International Journal of Applied Engineering Research 10.ISSN 0973-4562 (2015): 7489-7496.

[8] JAIGANESH, R. "Smart Grid System for Water Pumping and Domestic Application using Arduino Controller." International Journal of Engineering Research & Technology (IJERT) 5.13 (2017): 583-588.

[9] Pau1l, M. Mano Raja, R. Mahalakshmi, M. Karuppasamypandiyan, A. Bhuvanesh, and R. Jai Ganesh. "Classification and Detection of Faults in Grid Connected Photovoltaic System."

[10] Ganesh, Rajendran Jai, et al. "Fault Identification and Islanding in DC Grid Connected PV System." Scientific Research Publishing 7.Circuits and Systems, 7, 2904-2915. (2016): 2904-2915.

[11] Jaiganesh, R., et al. "Smart Grid System for Water Pumping and Domestic Application Using Arduino Controller." International Journal for Modern Trends in Science and Technology 3.05 (2017): 385-390.

[12] Kalavalli,C., et al. "Single Phase Bidirectional PWM Converter for Microgrid System." International Journal of Engineering and Technology (IJET) ISSN : 0975-4024 Vol 5 No 3 Jun-Jul 2013.

[13] Lilly Renuka, R., et al. "Power Quality Enhancement Using VSI Based STATCOM for SEIG Feeding Non Linear Loads. " International Journal of Engineering and Applied Sciences (IJEAS) ISSN: 2394-3661, Volume-2, Issue-5, May 2015.

[14] Karthikeyan,B. JEBASALMA. "RESONANT PWM ZVZCS DC TO DC CONVERTERS FOR RENEWABLE ENERGY APPLICATIONS ." International Journal of Power Control and Computation(IJPCSC)Vol 6. No.2 – Jan-March 2014 Pp. 82-89 ©gopalax Journals, Singapore available at : www.ijcns.com ISSN: 0976-268X.

[15] Gowri,N, et al. "Power Factor Correction Based Bridgeless Single Switch SEPIC Converter Fed BLDC

[16] Motor." ADVANCES in NATURAL and APPLIED SCIENCES. ISSN: 1995-0772 AENSI Publication EISSN: 1998-1090 http://www.aensiweb.com/ANAS 2016 March 10(3): pages 190-197.

[17] Ramkumar,R., et al." A Novel Low Cost Three Arm Ac Automatic Voltage Regulator" ADVANCES in NATURAL and APPLIED SCIENCES ISSN: 1995-0772 AENSI Publication EISSN: 1998-1090 http://www.aensiweb.com/ANAS 2016 March 10(3): pages 142-151.

[18] Raguraman, L., and P. Sabarish. "Integrated Bridgeless PWM Based Power Converters." International Journal of Advanced Research in Engineering & Technology (IJARET) 4.5 (2013): 17-23.