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Boosting Inverter Without electrolytic capacitor In a Single Stage Conversion

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Abstract : *This paper introduces a high-gain single-stage boosting inverter for alternative energy generation. As compared to the traditional two-stage approach, the SSBI has a simpler topology and a lower component count. One cycle control was employed to generate ac voltage output. This paper presents theoretical analysis, simulation and experimental results obtained from a 200 W prototype. The experimental results reveal that the proposed SSBI can achieve high dc input voltage boosting, good dc–ac power decoupling, good quality of ac output waveform, and good conversion efficiency.*

Keywords - *OCC-One cycle control, TI-tapped inductor, SSBI- single-stage boosting inverter*

I. INTRODUCTION

Microinverter topologies for photovoltaic (PV) power generation are classified into three major groups the single-stage, the two-stage, and the multi-stage types. The multistage micro inverters are usually comprised of a step-up dc–dc converter front stage, under maximum power point tracking (MPPT) control, an intermediate high-frequency dc–dc converter stage, used to attain a rectified-sine waveform, and a low frequency unfolding stage to interconnect to the grid [2],[3]. However, the multistage power train and the associated high component count result in a costly product [4]. The two-stage microinverter can be designed cascading a MPPT-controlled step-up dc–dc converter and a grid-tied high-frequency inverter, whereas the single-stage topology has to perform the voltage step up, the MPP tracking, and the dc–ac inversion functions all in one stage.

In order to convert and connect the solar energy to the grid, the low voltage of the PV panel first has to be stepped up significantly to match the utility level. This poses a challenge to the designer of PV inverters as the traditional boost converter cannot provide the required gain at high efficiency. Therefore, an extensive research effort is dedicated to developing various topologies of high step-up dc–dc converters [5]–[7] that can be used in tandem with a half- or full-bridge inverter [8] to implement a solar power generation system.

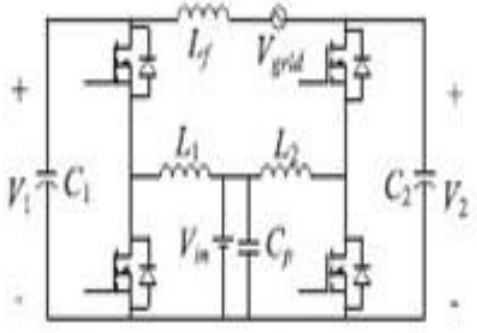


Fig 1(a).Topology presented in olden techniques

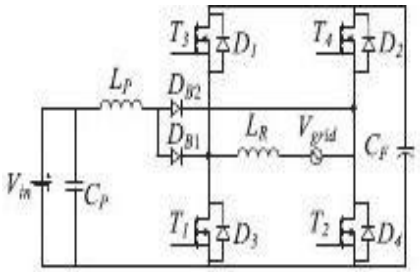


Fig 2.Topology presented in Convetional

Another concern, typical to single-phase dc–ac power systems, is ac–dc power decoupling problem. A traditional solution is application of a decoupling capacitor on the dc-link between the input and output stages. The value of the decoupling capacitor depends on the rated power Pdc , the line frequency f, the average voltage across the capacitor Vdc , and the allowed peak-to-peak ripple Δv. The two-stage or the multistage microinverters can have their decoupling capacitor on the high voltage dc link, and, according to it, attain lower value of the decoupling capacitor . However, some single stage microinverters may require placing the decoupling capacitor at the PV module terminals. The low panel voltage, Vdc , and the desired low ripple, Δv, result in a substantial decoupling capacitor value and size (e.g., 2.4 mF for Vdc = 35 V, Δv = 6 V, and Pdc = 160 W). In field conditions, large electrolytic capacitors have short life and impair system's reliability [1] and [6].

Therefore, the power decoupling problem becomes one of major concerns in micro inverter design. Application of small non-electrolytic capacitors is strongly desired. To minimize the decoupling capacitor, additional power decoupling circuits were suggested in literature. A flyback-type single-stage topology with an additional power decoupling circuit proposed in reported a decoupling capacitor of only 40 μF. However, the efficiency was only 70%. An improved topology employing leakage energy recycling demonstrated 86% peak efficiency. Some other fly back-based topologies and also make use of an additional power decoupling circuit.

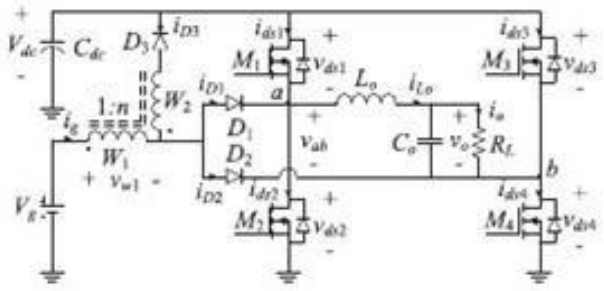


Fig 3.Topology presented in SSIB

Single-stage topologies that can realize voltage step-up and inversion in a single stage were proposed in the past. In , adual boost inverter was suggested. Here, the load is connected differentially between the outputs of two bidirectional boost converters (see Fig. 1). As a result, the topology resembles a common H-bridge with the boosting inductors connected to the legs' midpoints. The demerits of this approach are the limited dc step-up gain; circulating currents, which impair the efficiency; and somewhat complicated control [10].

Since the function of C1 and C2 is merely output filtering, the decoupling capacitor should be placed at the low voltage input, which is an additional disadvantage. Another single stage solution is shown in Fig. 2. Compared to the conventional topologies ,It use a single boost inductor; have no circulating currents; have a high voltage dc link and, accordingly, a smaller decoupling capacitor. Also, traditional control methods can be applied.

Moreover, the topologies proposed in the reference papers, It may provide other choices for single-

stage solutions. However, the limited dc step up of the necessitates using a more expensive high-voltage PV panels with 70–100 VDC output in order to get the desired dc-bus voltage compatible to grid-connected inverters. Alternatively, using the popular crystalline silicon modules with the 25–50 VDC MPP range, these topologies can implement a two-three panel string inverter, which, as any string architecture, is prone to the mismatch problem.

In this paper, a single-stage boosting inverter (SSBI) is proposed for alternative energy/solar power generation. SSBI can be regarded as further improvement in it. SSBI can attain higher dc gain and, thus, operate off low dc input voltageof a single PV panel. By its concept of operation SSBI shares the switches of the power train in a manner that allows merging the dc–dc step-up converter stage and the grid-tied dc–ac inverter stage. Hence, SSBI is realized in a single stage. The power decoupling is performed at high voltage; thus, low value of dc-link decoupling capacitor is required[14].

The SSBI easily lends itself to application of one cycle control , which helps attaining high-quality ac output regardless of low frequency ripple across the dc link. However, any other control method can be applied. This paper presents theoretical analysis, simulation and experimental results obtained from a stand-alone 200 W prototype.

II. DESCRIPTION OF THE PROPOSED TOPOLOGY

The proposed schematic diagram of the proposed SSBI is given in Fig. 3, which is an improvement of the scheme given in [16] . SSBI is comprised of semiconductor switches M1 . . . 4 , arranged in a full-bridge configuration; steering diodes D1, 2 ; dc-link diode D3 , the tapped inductor (TI) W1 :W2 ; the decoupling capacitor Cdc ; and the output filter Lo − Co . The load is represented by the resistor RL . The proposed SSBI is fed by a dc voltage source, Vg , considered to be derived of a single PV panel, and generates utility level ac output voltage Vo . Here, the input current is designated as ig , the output current is io and its average component is Io .

Compared to [16] , the proposed SSBI topology has the advantages of a larger voltage stepup which can be achieved adjusting the TI turns ratio, and smaller decoupling capacitor, which is placed on high voltage dc bus. Principle of operation of the proposed SSBI is hinged on implementation of a specialized switching pattern of the H-bridge. In order to generate output voltage of positive polarity, three topological states are created during the switching cycle as shown in Fig. 4. Here, buck and boost sub topologies can be identified.

The switching cycle starts with State A, shown in Fig. 4(a), which lasts for a duration of ta . Here, the switches M1 and M4 are ON, whereas switches M2 and M3 are OFF, D2 conducts and D1 , D3 are cut-off. During this state, the TI primary magnetizing inductance Lm is charged from the input voltage source Vg , while the dc voltage Vdc is applied to the input terminals of the output filter so the filter inductance Lo is charged feeding also the filter capacitor Co and the load RL .

State B [see Fig. 4(b)] commences, as the switch M1 is turned off and M2 is turned on, whereas M4 keeps conducting. State B

lasts for a duration of tb . Here, both D1 and D2 conduct while D3 is cut-off. As a result, the TI magnetizing inductance Lm continues charging from the input voltage source Vg , whereas the input terminals of the output filter are shorted so the filterinductance Lo is discharged to the output capacitor Co and the load RL .

TABLE I
SWITCHING STATES OF SEMICONDUCTOR DEVICES

	Positive output voltage			Negative output voltage		
	State A	State B	State C	State A	State B	State C
M_1	ON	OFF	ON	OFF	OFF	ON
M_2	OFF	ON	OFF	ON	ON	OFF
M_3	OFF	OFF	ON	ON	OFF	ON
M_4	ON	ON	OFF	OFF	ON	OFF
D_1	OFF	ON	OFF	ON	ON	OFF
D_2	ON	ON	OFF	OFF	ON	OFF
D_3	OFF	OFF	ON	OFF	OFF	ON

State C [see Fig. 4(c)] begins as the switches M1 , M3 are turned on and M2 , M4 are turned off. State C lasts for duration of tc , and completes the switching cycle. Here, both D1 , D2 are cut-off and D3 conducts; the TI magnetizing inductance Lm is discharged via both windings and D3 into the dc-link capacitor Cdc , while the input terminals of the output filter are shorted and the filter inductance Lo feeds the output capacitor Co and the load RL .

In order to generate output voltage of negative polarity, complementary switching states A , B , and C are created by the controller. Switching states of semiconductor devices throughout the switching cycle are summarized in Table I. To create the desired switching states, proper switching signals for the H-bridge switches should be generated of the given buck and boost switching functions and the output polarity signal Sbk (Dbk), Sbst (Dbst), P, respectively. Here, the driving signals of the switches M1 . . . M4 are designated as S1 . . .S4 , respectively. The required Boolean functions can be derived from Table I.

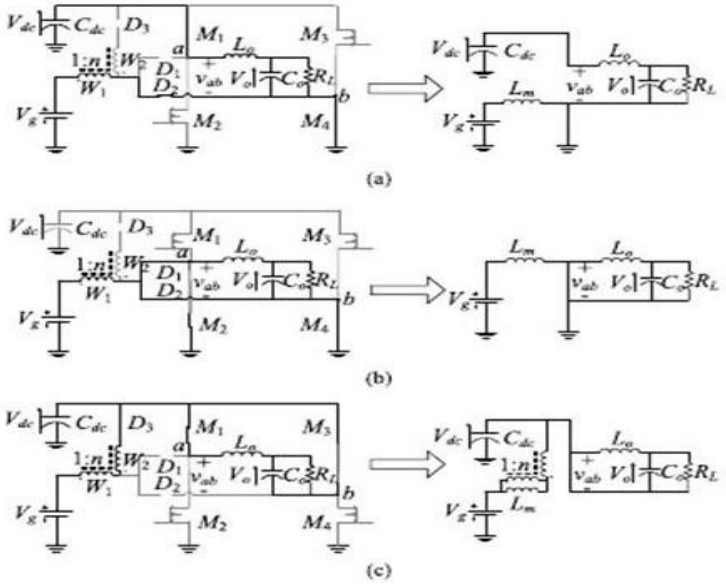


Fig 4.Topological states of the proposed SSBI

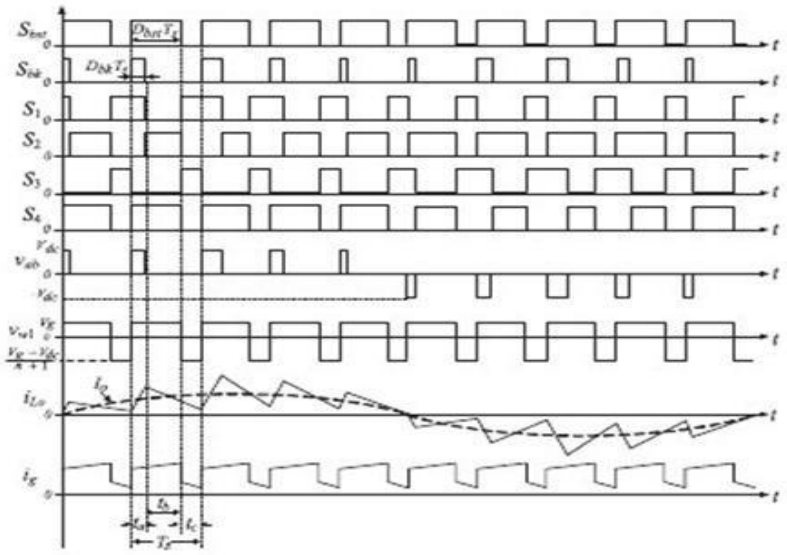


Fig 5. Key waveforms of the proposed SSBI.

Key waveforms of the proposed SSBI throughout a line frequency cycle are illustrated in Fig. 5. Note that since the switching cycle of SSBI is comprised of three states, there are 3! possible permutations or state sequences. In other words, the order of appearance of the states is not unique and other possibilities exist, i. e. A–C–B, C–B–A, etc. An ideal SSBI can generate same dc–dc conversion ratio under any of these switching

regimes. However, some state sequences may require switches to be activated twice per switching cycle,which is undesirable in practice due to increased switching loss and/or extremely narrow on time. Proper synchronization of the gating signals also requires attention. The advantage of the implemented A–B–C state sequence is that each switch is turned on and off only once in a switching cycle, which helps reducing the switching losses.[11]

$$S_1 = P \cdot \overline{S_{bk} \cdot S_{bst}}$$
$$S_2 = P \cdot \overline{S_{bk} \cdot S_{bst}}$$
$$S_3 = P \cdot \overline{\overline{S_{bk}} \cdot S_{bst}}$$
$$S_4 = P \cdot \overline{\overline{S_{bk}} \cdot \overline{S_{bst}}}, \qquad \text{.....(1)}$$

As a result of the proposed switching strategy, the voltage Vab at the input terminals of the output filter is a three-level pulse train, which can be properly modulated to generate the desired output waveform of either polarity as shown in Fig. 5.

III. SSBI ANALYSIS AND SIMULATION

To facilitate the analysis approach, the following assumptions are adopted: 1) all semiconductors are ideal with zero on resistance and voltage drop; 2) the decoupling capacitor and the output filter capacitor are sufficiently large and their voltage ripple is negligible; and 3) continuous current operation of both the TI TI and the output filter inductor is assumed[13].

A. Derivation of Voltage Conversion Ratio

Inspection of the converter's equivalent circuits in Fig. 4 reveals that the power stage operates as a boost-derived TI dc–dc converter merged with a buck-derived full-bridge dc–ac inverter. Define ta , tb , and tc the duration of states A, B, and C, respectively, and Ts = ta + tb + tc the switching period. Boost charging state, that is the time interval dedicated to charging the primary winding of the TI, takes place during states A and B [see Fig. 4(a) and (b)] whereas boost discharge takes place in state C. The total duration of the boost charging is therefore Hence, SSBI performs the dc–dc step-up conversion function identically to the TI boost converter. Adopting the approach of authors in [12] , the dc–dc voltage conversion ratio of tbst = ta + tb.....(2)

Accordingly, the resulting boost duty cycle D_{bst} is

$$D_{bst} = (ta + tb)/ Ts \ldots\ldots(3)$$

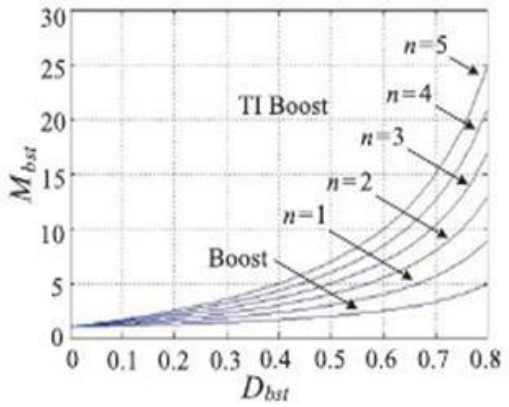


Fig. 6. Comparison of conversion ratio, M_{bst} , of the traditional boost and the TI boost converters.

SSBI is

$$M_{bst} = \frac{Vdc1 + nD_{bst}}{Vg1 - D_{bst}} \quad \text{.....(4)}$$

The voltage conversion ratio (5) is plotted in Fig. 6. Clearly, by adjusting the turn ratio, n, the proposed SSBI can achieve higher conversion ratio than a traditional boost converter. According to the aforementioned state description, the buck charging state, that is, the time interval dedicated to charging the output inductor, Lo , occurs in state A, whereas buck discharge
takes place in states B and C while the terminals of the output filter are shorted. Thus, the duration of the buck charging is

$$t_{bk} = t_a \text{ ..... (5)}$$

Clearly, under CCM condition of the output filter inductor, the voltage gain of the output section is identical to that of a buck converter and is given by

$$Mbk = Vo / D_{bst} \text{ ..... (6)}$$

In stand-alone application, the buck duty ratio Dbk is modulated to attain a sinusoidal output voltage Vo of required amplitude and frequency, whereas the boost duty ratio Dbst is adjusted to satisfy load power demand and so stabilize the dc-link voltage Vdc . However, an important constrain arising from SSBI principle of operation is that the buck duty ratio Dbk should be smaller than the boost duty ratio Dbst at all times: Dbk < Dbst .

B. Voltage and Current Stress of Semiconductor Devices

Peak voltage and peak current of the semiconductor devices during a switching cycle are summarized in Table II. The values of the RMS currents of the semiconductor devices throughout the line cycle are given in Table III. Here, the√RMS value of buck duty cycle is defined as Dbkrm s = Dbkm / 2.

C. Simulation Results

A stand-alone variant of the proposed SSBI and its OCC control circuits was implemented for preliminary study using PSIM
Version 9.1 software. Simulation waveforms in Fig. 7 reveal the details of SSBI operation on the switching frequency scale,
which support the theoretical predictions.

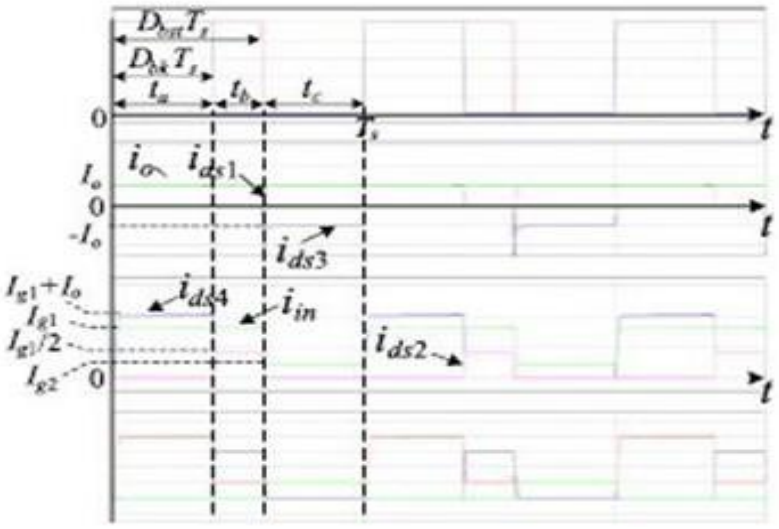


Fig. 7. Simulated waveforms of the proposed SSBI on the switching frequency scale during positive half-cycle.

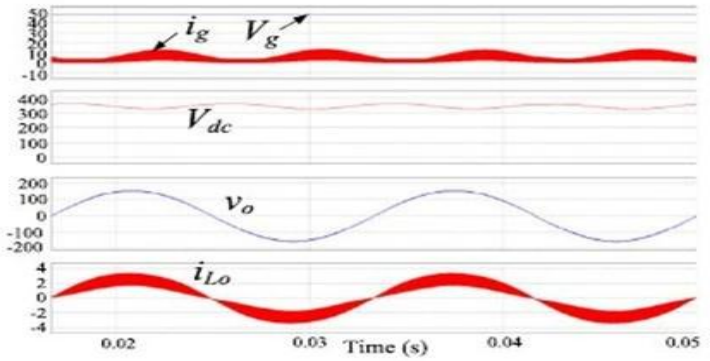


Fig 8.Simulated waveforms of the proposed SSBI on the line frequency

Fig. 8 illustrates the principal SSBI waveforms on line frequency scale and confirms that under the OCC control the proposed SSBI can provide high dc input voltage stepup as well as high-quality ac output. The advantage of the OCC control can be now clearly observed: due to the superior transient response of the OCC controller, the substantial ripple component of the dc-link voltage has no detrimental effect on the quality of the ac output. Hence, lower decoupling capacitor can be employed without compromising dc–ac decoupling. Another advantage of the proposed approach is that the OCC controller required no sensing of the ac output voltage. Hence, there is no need for isolated floating sensors, which further simplifies the circuitry. Detailed description of OCC controller can be found in [16] and [12].

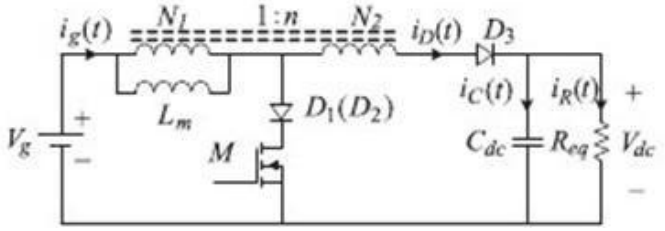
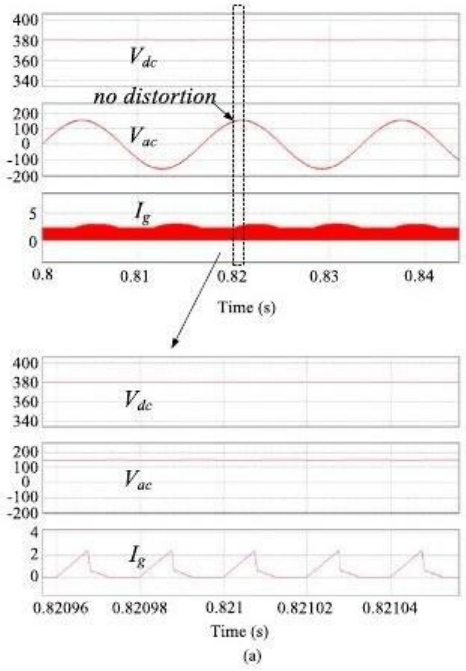


Fig. 9. Input voltage step-up scheme of the proposed SSBI (is identical to the TI boost converter).



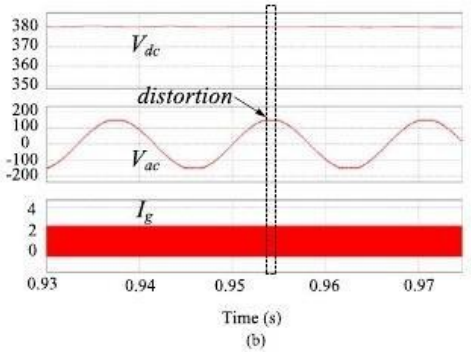


Fig. 10. Simulated waveforms of the SSBI's output voltage V a c , dc-link voltage V d c , and dc input source current Ig : (a) illustrating the undistorted output voltage V a c , when SSBI is operated in deep DCM just above the minimumpower level P o > P o m in and (b) illustrating the peak-shaving distortion of the output voltage V a c for P o < P o min .

The boost duty cycle Dbst is plotted as function of the output power Po in Fig. 11 for the following set of parameters: Vg = 48 V, Vdc = 380 V, n = 3, Lm = 150 μH, and Ts = 20 μs. Evidently, Dbst is constant in CCM and, according to (5) equals Dbst (CCM) = 0.64. The DCM duty cycle can be calculated from the Dbst = 0.0057Po . The DCM–CCM boundary power Pob = 68.36 W was calculated from it.Fig. 11 also illustrates that the Dbst = Dbkm condition occurs at the minimum output power Pom in . Under lighter loading,

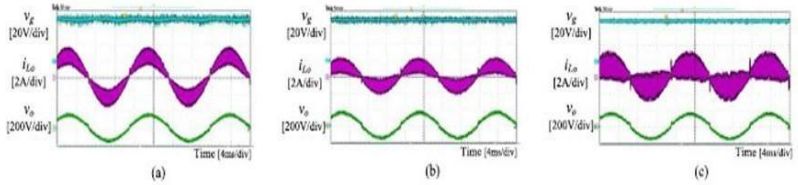


Fig 11.Experiment results of v g , iLo, v o under different output power (V g = 48 VDC): (a)200W,(b)100 W, (c) 50 W

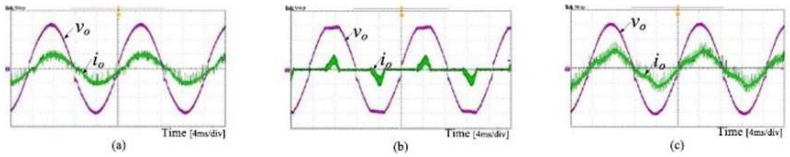


Fig. 12. Experimental results: SSBI's output voltage v o and output current io under three different load conditions: (a) linear RL load, (b) nonlinear load case I: diode bridge with RC load, and (c) nonlinear load case II: resistor and saturable inductor load.

D. Verification of DCM Analysis

PSIM simulation was used to verify the DCM voltage conversion ratio (15). The simulation parameters were as follows:Vg = 48 V, Lm = 150 μH, Ts = 20 μs, Dbst = 0.64, n = 3,and Req = 4000 Ω. Plugging these parameters into (15) yields Mcal = 10.96, whereas the simulated result is Msim = 10.58 strongly supporting the theoretical expectation.

The CCM–DCM boundary condition (16) was verified by simulation using the following parameters: Vg = 48 V, Lm =150 μH, Ts = 20 μs, Dbst = 0.64, and n = 3. The exploded view of the input current Ig (shown in Fig. 12) clearly indicates that SSBI is indeed at the CCM–DCM boundary. The simulated output power was found as Pob = 67 W and matched the theoretically expected value of Pob = 68.36 W calculated.

IV. EXPERIMENTAL RESULTS

Experimental stand-alone prototype SSBI was built and tested. The prototype was designed for a 200 W power output, 35–48 V dc input, and 110 V ac output voltage. The switching frequency was set to 50 kHz. The OCC controller and timing circuits were implemented using standard analog and logic chips. The key

components of the SSBI prototype were M1 –M4 :SCT2080KE; D1 –D2 : STTH30L06; D3 : C3D04065A; decoupling capacitor Cdc : 47 μF//450 V; TI turns ratio were as follows: 1:3 for the 48 V input unit and 1:4 for the 35 V input unit, magnetizing inductance 150 μH; output filter inductance Lo :1 mH; output filter capacitance Co : 1.5 μF; Magnetics' cores: C058439A2 and C058254A2 were used. Boost signals were generated with a simple PWM controller UC3824. Fast comparator AD8561 was used to implement the OCC. The experimental work was aimed to verify the principles of the proposed approach. No optimization was attempted.

The experimental waveforms are presented in Figs. 14 and 17. Fig. 14 shows the waveforms of input and output voltage,along with the output inductor current. The measurements were taken at three different power levels at constant input voltage. SSBI generated high-quality ac output voltage in a wide range of output power. Several different load types were presented to SSBI. Fig. 15 shows the waveforms of the output voltage and output current under three different load conditions: 1) linear RL load; 2) nonlinear load case I: diode bridge with RC load; and 3) nonlinear load case II: resistor and a saturable reactor load. The measured total harmonic distortion (THD) of the output voltage was 4.98%, 8.5%, and 4%, respectively.

V. CONCLUSION

A high-gain SSBI for alternative energy generation applications is presented in this paper. The proposed topology employs a TI to attain high-input voltage stepup and, consequently, allows operation from low dc input voltage. This paper presented principles of operation, theoretical analysis of continuous and discontinuous modes including gain and voltage and current stresses. To facilitate this report, two stand-alone prototypes one for 48 V input and another for 35 V input were built and experimentally tested. Theoretical findings stand in good agreement with simulation and experimental results. Acceptable efficiency was attained with low-voltage input source. The proposed SSBI topology has the advantage of high voltage stepup which can be further increased adjusting the TI turns ratio. The SSBI allows decoupled control functions. By adjusting the boost duty cycle Dbst , the SSBI can control the dc-link voltage, whereas the output waveform can be shaped by varying the buck duty cycle Dbk .The ac–dc power decoupling is attained on the high-voltage dc link and therefore requires a relatively low capacitance value. highly nonlinear loads.

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