Journal of Science and Technology
ISSN: 2456-5660, Volume 5, Issue 3, May-June 2020

www.jst.org.in *DOI: https://doi.org/10.46243/jst.2020.v5.i3.pp01-08*

Design and Implementation of Programmable Logic Array Using Quantum Dot Cellular Automata

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To Cite this Article

Ashwini Mane, Shubham Pansare, Pratiksha Rupnawar, Dr.Varsha Harpale and Dr.Deepti Khurge, "Design and Implementation of Programmable Logic Array Using Quantum Dot Cellular Automata", Journal of Science and Technology, Vol. 05, Issue 03, May-June 2020, pp01-08

Article Info

Received: 25-01-2020 Revised: 15-04-2020 Accepted: 20-04-2020 Published: 24-04-2020

Abstract :*Quantum Dot Cellular Automata (QCA) is an alternative to CMOS technology. The other technologies proposed by researchers are FINFET, CNTs and MTJ to reduce scalability of CMOS devices. Using Quantum Dot Cellular Automata, the low power, extremely dense circuits are designed. QCA cell is the fundamental unit in building logic gates. These cells are powered using specific clock. QCA cells are used to design basic gates and to realize Boolean expressions. QCA Designer tool is used to carry out simulations. The simulation results are same as theoretical results. The complexity and size of circuits are reduced using QCA. The paper includes design of Programmable Logic Array (PLA).*

Keywords:*Boolean Expression, Clock, CMOS, Fundamental Unit, QCA Designer*

I. Introduction

According to Moore's law, the number of transistors doubles every 18 months in CMOS circuits. New technologies are emerging due to various problems faced by the current transistor technology like high power dissipation and size reduction.Many parameters have changed due to integration. There is limit to scale various devices so new emerging technologies have been emerging like FINFET,CNTs, MTJ and QCA. Quantum Dot Cellular technology (QCA) is emerging nano-scale technology. QCA is fundamental unit of QCA. QCA cell consists of two electrons which occupy diagonal position due to electrostatic repulsion. When two cells are brought together they occupy same polarization. They change the state immediately if one of the cell changes the polarity.

II. Important Terminologies

2.1 QCA Cell

QCA is operated through QCA cells, also called quadratic cells. QCA cell consists of four quantum dots situated at four corners of a square structure in which each dot is capable of holding one electron. The quantum dots are connected to each other through the tunneling junctions. The electrons can travel across the quantum dots using these tunnel junctions, also called as electron tunnel junctions. In QCA cell, only two electrons are injected. The two electrons will move towards the two diagonally opposite corners due to columbic forces interacting between them. There are two ways in which the electrons will occupy the diagonal positions leading to formation of two polarizations -1 and +1 representing Binary 0 and Binary 1 respectively as shown in Fig. 1 and 2. By giving a clock signal, these electrons can travel through the tunnel junctions.

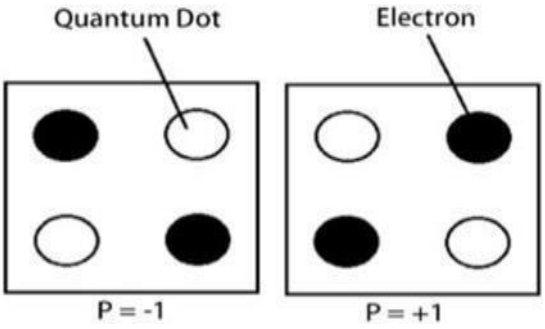

Fig. 1:Structure of QCA cell [1]

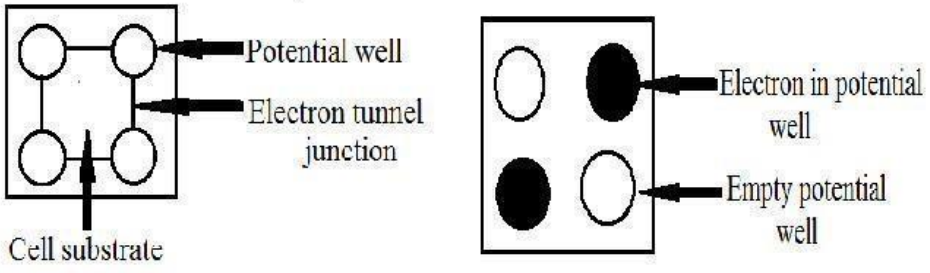

Fig. 2: Potential Well in QCA [1]

2.2 QCA Wire

Several QCA cells when placed one after the other in a serial manner leads to the formation of QCA wire. Binary information from one cell is passed to other cell due to columbic interaction between the cells. If the first cell adjacent to other cell holds a certain state, then the adjacent cell will be forced to have same state in order to lower its energy. Different ways of orientation of QCA cells in wire results into two types of QCA wire. In 90 degree aligned QCA wire, polarization of the input cell is propagated down the wire whereas in 45 degree aligned QCA wire, output is the negotiated version of the polarization given to input cell.

2.3 Majority Gate

The majority gate consists of 5 cells arranged in a manner as shown in Fig. 3. Out of these 5 cells, 3 cells are input driven and hence also known as 3 input majority gate. The equation for a majority gate is M (A, B, C) = AB+BC+AC). Depending upon the three inputs and majority consideration, the polarization of central cell is done which is then propagated as the output. By fixing one of the input as a constant(0 or 1), AND and OR gates can be implemented. If the input is set to logic 1, then OR gate is implemented and by setting the input to logic 0, AND gate is implemented.

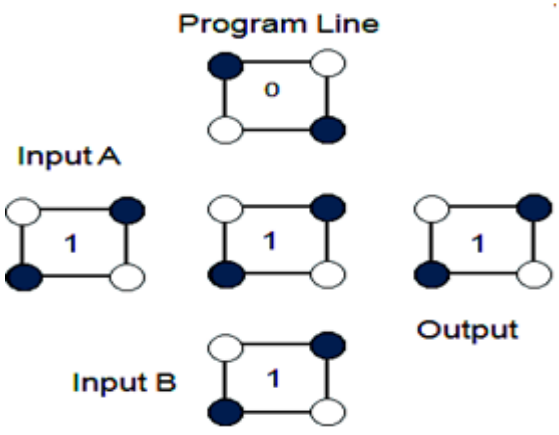

Fig. 3 : Structure of Majority Gate[8]

2.4 QCA Clock

Since there is no external power source for running the QCA circuits, clock provides the power to run the circuits besides its use for controlling signal propagation and synchronization purpose. The clock is divided into four phases for proper operation and functioning of it such as SWTICH, HOLD, RELEASE and RELAX. It is assumed to have 90-degree phase lag between the two phases. Further there are four states of clock signal like high-to-low, low, low-to-high and high. During high-to-low state, the cell computation begins and it holds the value during low state. During low-to-high state, the cell is released and inactive during high state.

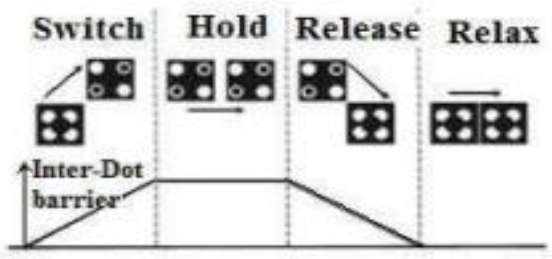

Fig. 4: Clock Phases in QCA Designer Tool [8]

2.5 QCA Inverter

When two cells are arranged diagonally then the output waveform is inverted.

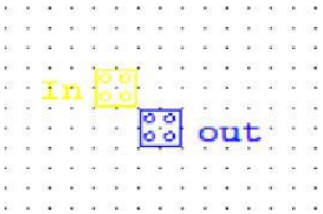

Fig. 5 : QCA inverter gate [1]

III. Implementation

3.1 Inverter

The output waveform of inverter is inverted.

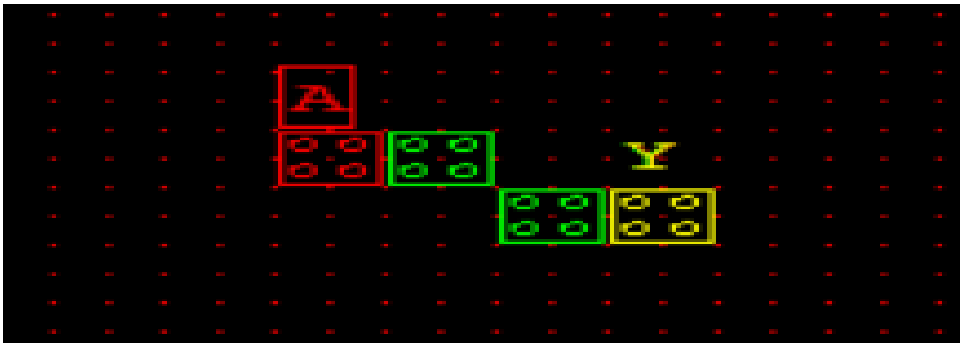

Fig. 6: Inverter Design in QCA Designer Tool

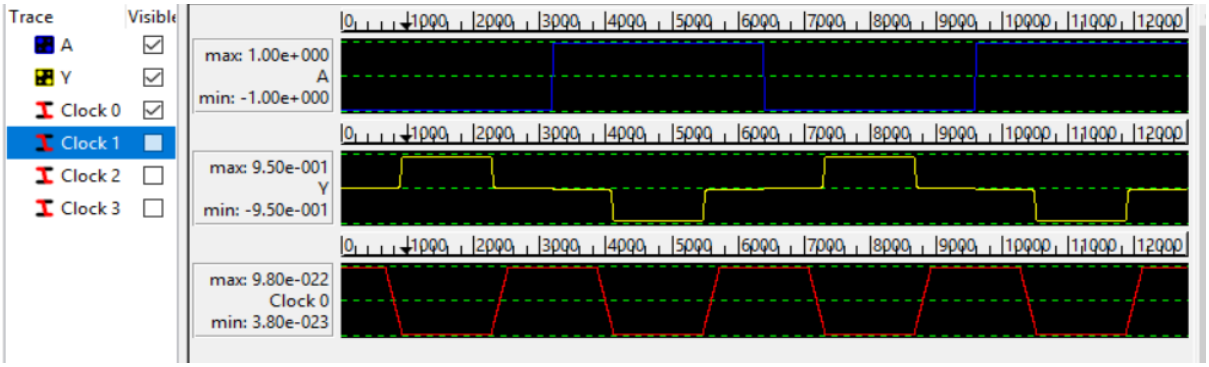

Fig. 7: Output Waveform of Inverter

3.2 Boolean Expression using QCA

Boolean Expression returns the values either true or false. The complicated Boolean Expressions can be simplified using algebraic rules. The equations can be reduced using by reducing number of terms or number of operations. This will increase reliability and reduce cost of manufacture. [7]

The two Boolean Expression are as follows:

$[(\overline{AB}) + (\overline{A+B})\ ].A\overline{B}$

$= [\overline{A} + \overline{B} + (\overline{A}.\overline{B})].A\overline{B}$ ……..De Morgan's Theorem

$=\overline{A}A\overline{B} + \overline{B}A\overline{B} + \overline{AB}A\,\overline{B}$

$=0+\overline{B}A+0$ ……...$\overline{A}A = 0$

$=\overline{B}A$ ……(1)

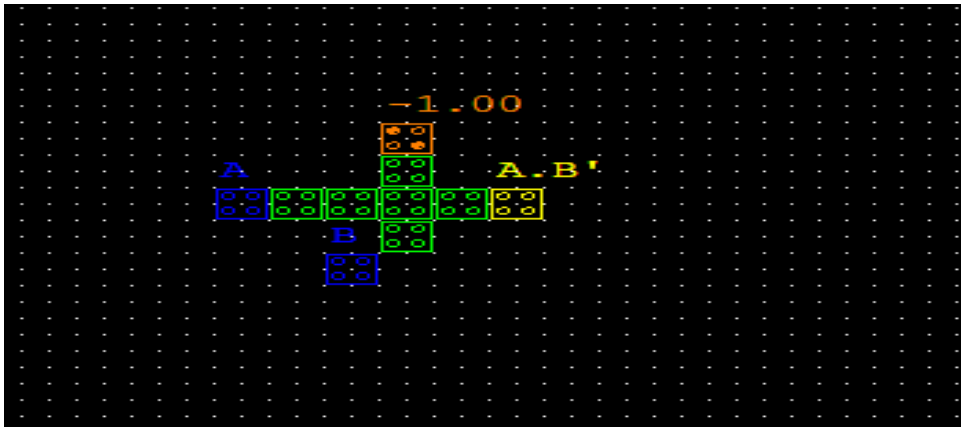

Fig. 8: Design for Boolean expression $[(\overline{AB}) + (\overline{A+B})\ ].A\overline{B}$ with output A.B'

Fig. 8 shows AB' which is the and operation of A and negation of B which is obtained by solving the Boolean expression.

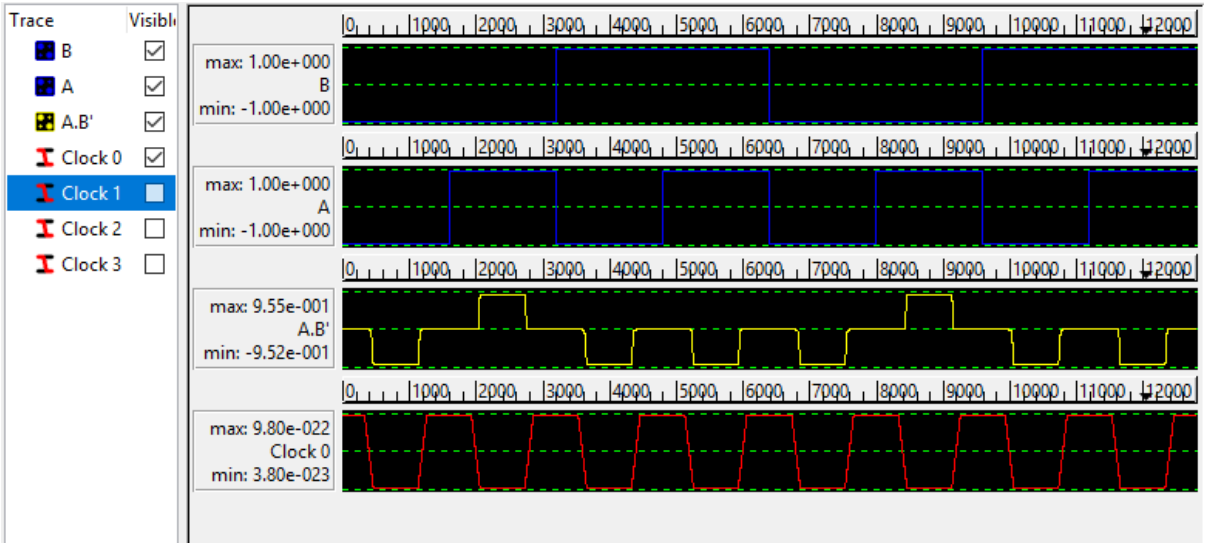

Fig. 9: Output waveform of Boolean Expression with output A.B'

In the Fig. 9 the output Y(X+Z) is obtained by first OR operation between X and Z. Then AND operation is performed between (X+Z) and Y. The waveforms were theoretically verified.

The second Boolean Expression is as follows:

$$XY + XYZ + XY\overline{Z} + \overline{X}YZ$$

$= XY + XY\overline{Z} + XYZ + \overline{X}YZ$

$= XY + XY\overline{Z} + XYZ + \overline{X}YZ$

$1 + \overline{Z} = 1$ $X + \overline{X} = 1$ ……...Boolean Expression Rules

=XY +YZ

=Y(X+Z) ……(2)

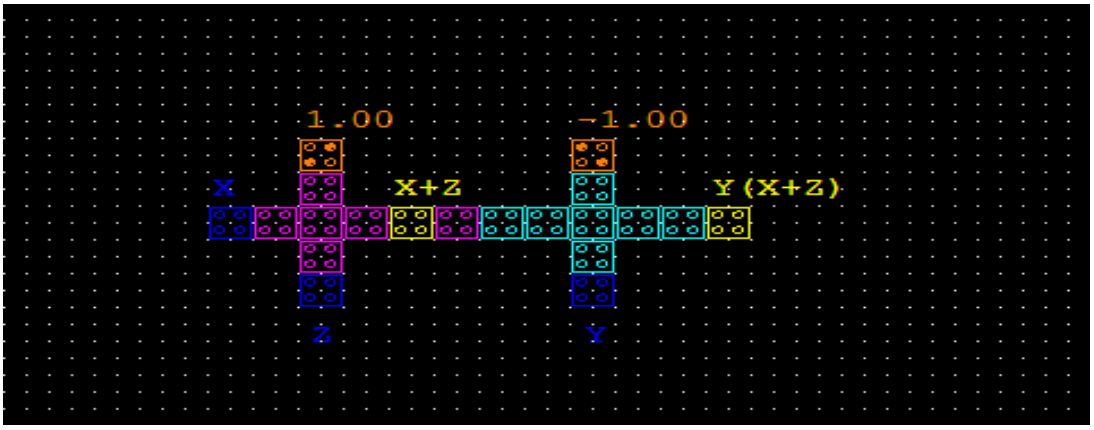

Fig. 10: Design for Boolean expression $XY + XYZ + XY\overline{Z} + \overline{X}YZ$ with output Y(X+Z)

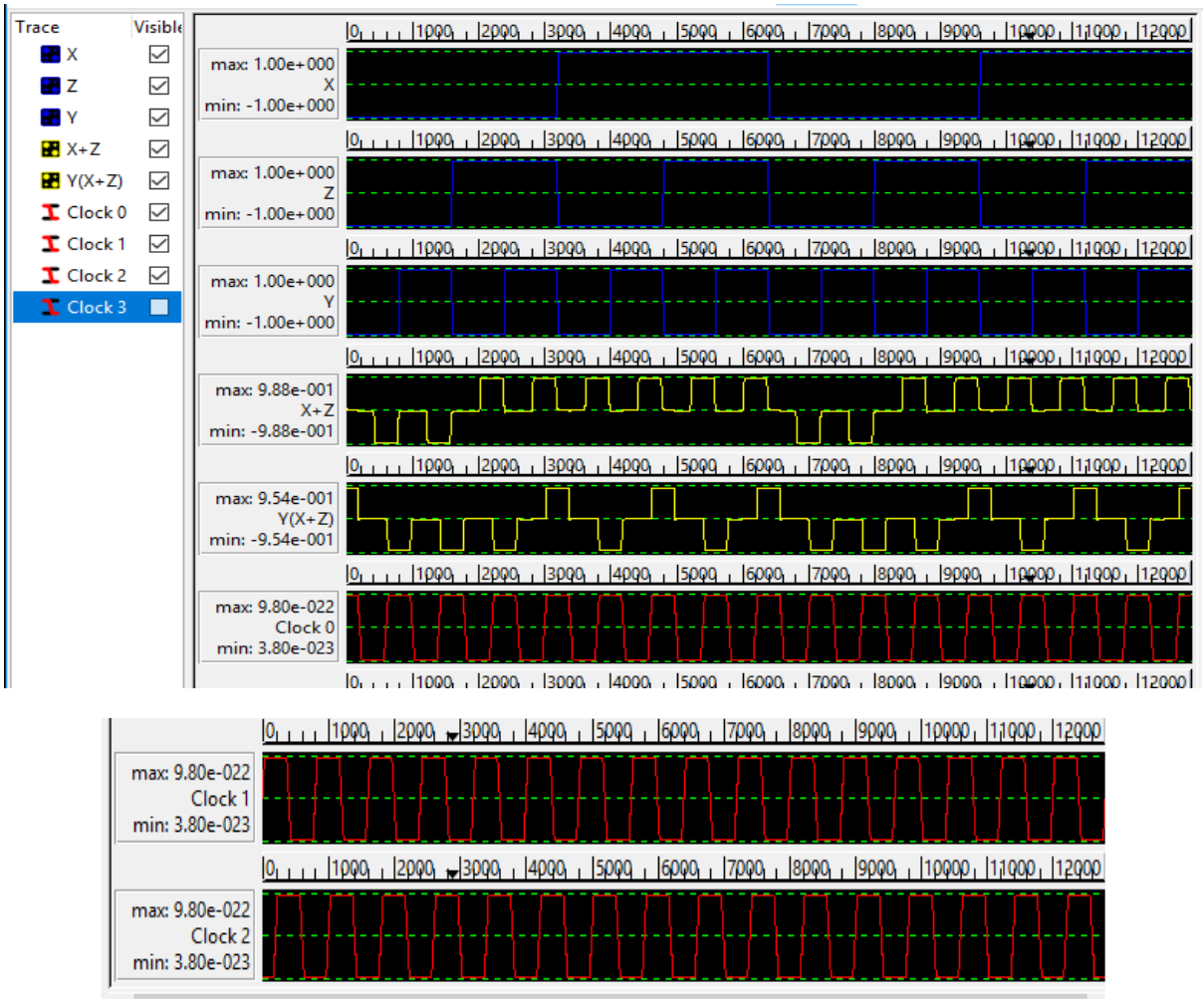

Fig. 11: Output waveform of Boolean Expression with output Y(X+Z)

3.3 PLA

Programmable logic devices (PLD) are the simplest, smallest and least-expensive forms of programmable logic devices. SPLDs can be used in boards to replace standard logic components (AND, OR, and NOT gates), This structure allows the implementation of logic functions in the sum-of-products form. PLAs are particularly useful for large designs that require many common product terms that can be used by several outputs. In Programmable Logic Array both the AND and OR array is programmable. The output of this is obtained as per our requirement. [6]. Fig. 15 shows the architecture of a simple PLA.

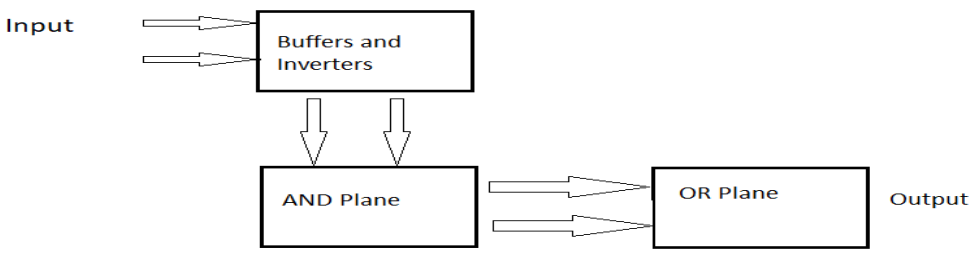

Fig. 12:Architecture of PLA

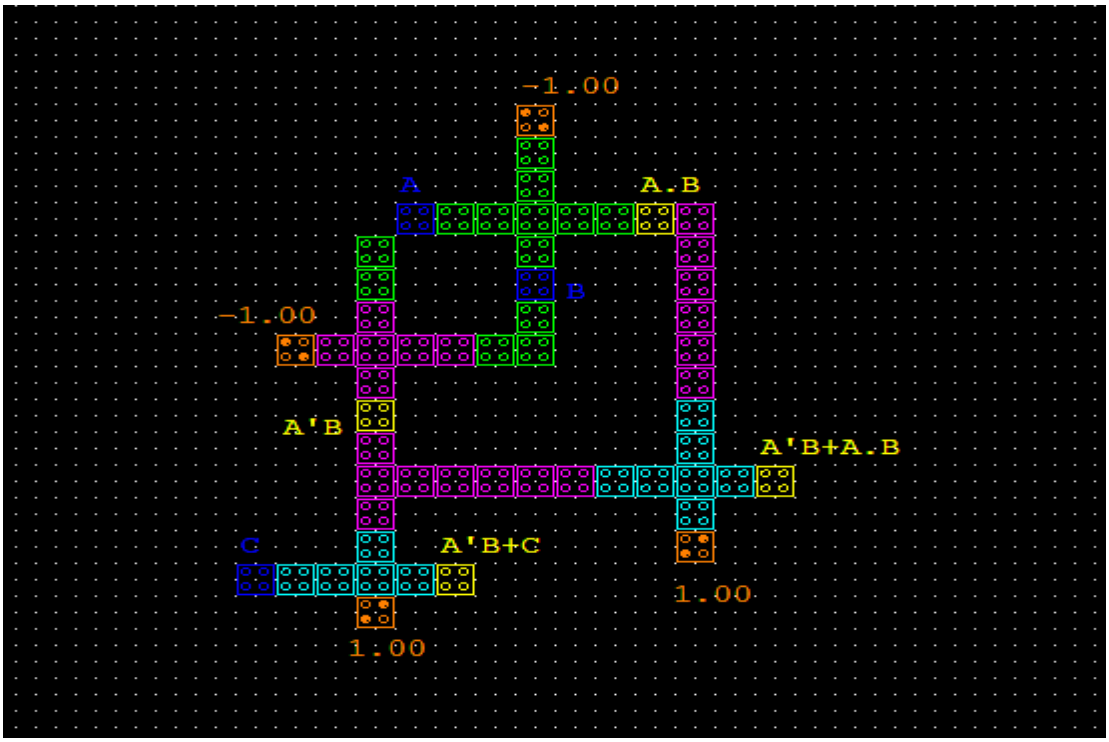

Fig. 13: Design of PLA in QCA Designer Tool

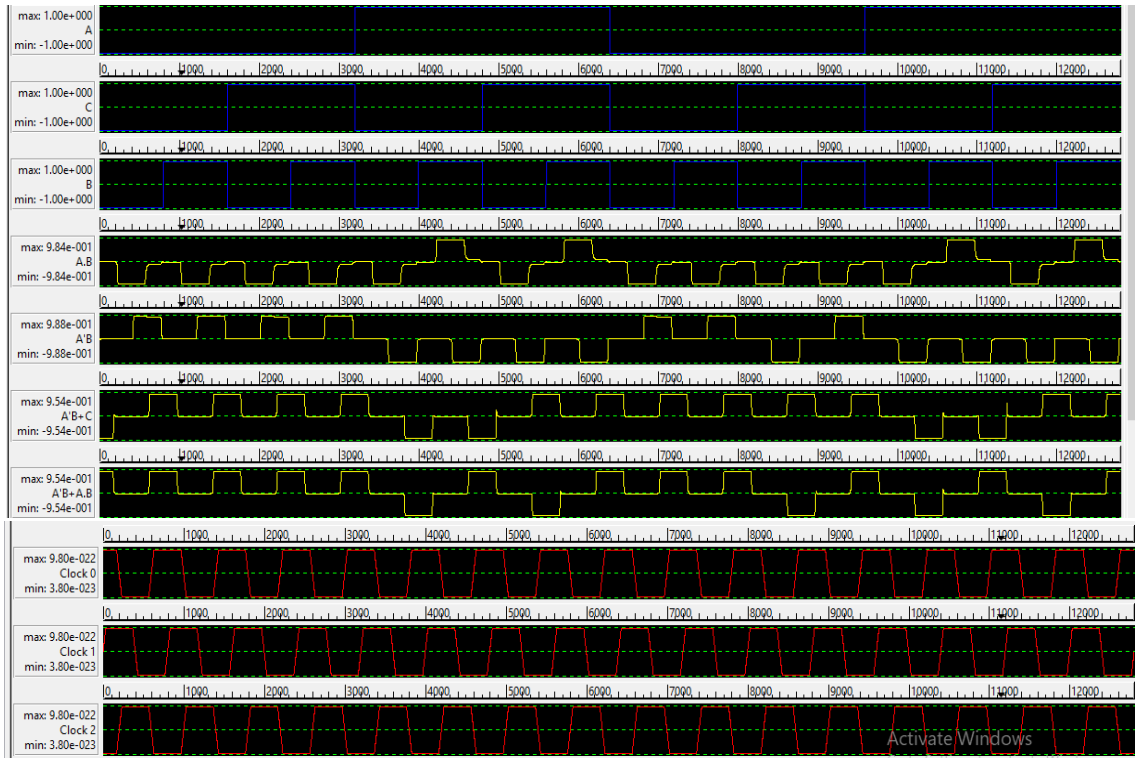

Fig. 14: Output of PLA

Three variables A, B, C are taken as input and two outputs A'B+C and A'B+A.B are obtained by using AND gate and OR gates.

IV. Result Table

Sr.No	Design Name	Number of cells required	Area of circuit	Processing Time
1	Boolean expression$[(\overline{AB}) + (\overline{A+B})\ ].A\overline{B}$	10	0.02 um^2	1sec
2	Boolean expression $XY + XYZ + XY\overline{Z} + \overline{X}YZ$	20	0.04 um^2	1sec
3	PLA	56	0.13 um^2	1sec

Table No.1: Results of Implemented circuits

V. Conclusion

QCA circuit design presents a new functional paradigm for quantum computing, and nano-technology. The proposed designs can be used to build arithmetic and logic units in quantum based computers. The Boolean expression are implemented and designed a Simple Programmable Logic Array using QCA designer tool. It is observed that as compared to other technology their performances are improved but QCA is not used because current semiconductors processes have not yet reached a point where mass production of devices with such a small features up to 20 nanometers ispossible. A number of challenges like choice of molecules, the design of proper interfacing mechanism remain to be solved before this method can be implemented. sThe simulation result obtained were same as that of theoretical results. The design may be further simplified by reducing the number of cells.

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