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A Novel 31 Level Inverter with Level Boosting Network to Improve Power Quality in Distribution Network

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Abstract— In this project, a new general cascaded multilevel inverter using developed H-bridges is proposed. The proposed topology requires a lesser number of dc voltage sources and power switches and consists of lower blocking voltage on switches, which results in decreased complexity and total cost of the inverter. These abilities obtained within comparing the proposed topology with the conventional topologies from aforementioned points of view. Moreover, a new algorithm to determine the magnitude of dc voltage sources is proposed. The performance and functional accuracy of the proposed topology using the new algorithm in generating all voltage levels for a 31-level inverter are confirmed by simulation and experimental results

Keywords— H-Bridge, MLI, 31 Level, Distribution System

I. INTRODUCTION

Multilevel-inverters (MLI) are designed for processes that require high Volt-Ampere rating and for applications which desire high power-quality waveforms [1]. Large instantaneous common-mode voltage appears across motor terminals in Pulse Width Modulation (PWM) controlled inverter. Multilevel inverters can overcome this problem as each switching device has low dV/dt per cycle. Also, the efficiency is high as they operate at much lower frequencies than PWM-controlled inverters resulting in lower switching losses. Voltage source inverters like MLI can achieve high voltage with low harmonics.

Different levels of voltage sources are used based on the configuration. Symmetric structure uses all voltage sources of same level, whereas asymmetric structure can use one of the following configurations
Unary configuration

- Binary configuration
- Ternary configuration

Selection of source configuration depends on the topology used and the desired voltage levels. By using Unary configuration we can build a fault tolerant system. On the other hand, by using Binary or Ternary configuration we can achieve higher output levels with optimal number of switching components. When the number of output level rises, the output voltage and current waveform resembles the sinusoidal waveform. Due to high number of levels, the harmonics distortion of output voltage waveform decreases. Lower dV/dt is observed in multilevel inverter as the switching occurs between lower voltage levels when matched to two-level inverter.

In this paper, we present a multilevel inverter to produce 31-level of output, in which the MOSFETs are operated at fundamental frequency [2]. This technique enables the value of THD to lie in the range specified by IEEE standard 519 without using active or passive filter. DC/AC converters, commonly known as voltage source inverter are widely used due to their higher efficiency, cost effectiveness and reduced size of passive filters. [3, 4]. Multiple types of topologies have been developed to meet the requirement of industries where in, inverters with different power ratings, frequency, size and voltage-levels are necessary.

Power semiconductor switching devices are controlled using gate signals generated by using modulation techniques such as Sinusoidal PWM, Space Vector Modulation, and Selective Harmonic Elimination (SHE). These switching techniques generate pulses in such a way that output waveform will be adjusted to the sinusoidal wave. Two-level inverter use PWM [5,6] which is effective in producing switch voltage /current waveform, the time average of which will be equal to the desired reference. Dead time, which is the waiting time to prevent shoot-through of inverter, should be considered. Dead time requirement increases the lower order harmonics.

First multilevel-inverter topology consisted of single phase inverter connected in series. This topology is widely known as cascaded H-bridge (CHB) inverter [7]. Later, an inverter named Neutral Point Clamped (NPC) was constructed using diodes connected to the neutral point; which was capable of producing multi-level output voltage by using a single DC voltage source [8]. Flying Capacitor (FC) inverter was made using several capacitors [9]. Above said topologies are widely known as “Classical Topologies”. In recent years, research is focused on reduced device count inverters which require new control techniques as shown in Fig. 1. A modular topology named Packed U-Cell (PUC) which uses trinary configured voltage source is developed. The number of active switches remain constant in this topology [10].

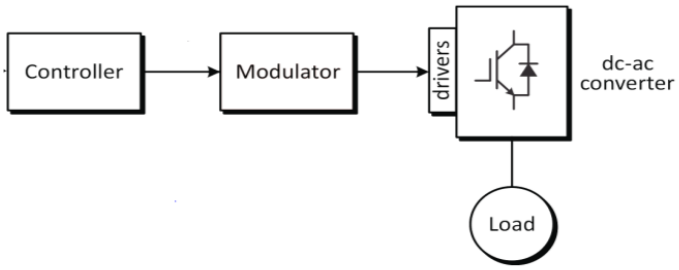

Fig. 1. Open-loop operation of DC/AC converter

II. MULTILEVEL INVERTER TOPOLOGY

Block diagram of the circuit to generate 31-level inverter output is given in Fig. 2 in which we have Level Generation Circuit and Polarity Generation Circuits which are controlled using control signals from Driving Circuit. Asymmetric structures have the ability to produce higher levels of output for similar quantity of semiconductor devices and voltage sources when compared to its symmetric equivalent. Fig.3 displays the MLI arrangement which is made up of asymmetric basic circuit called Level generator unit and an H-bridge inverter circuit called Polarity generation circuit. Stress on the switches in the polarity generation circuit will be higher compared to that of level generation unit.

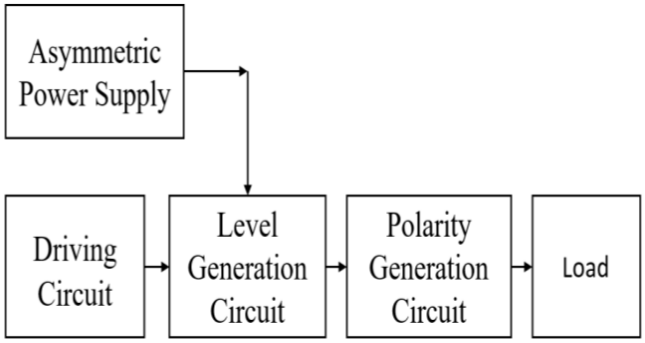

Fig. 2. Control block diagram

All the semiconductor switching components used in this circuit are unidirectional; due to that the number of MOSFETs and driver circuits remains the same. Current, blocking voltage, and switching frequency are the parameters which determine the amount of switching losses in multilevel inverter circuit. Table 1 gives us the status of each switch in the level generation unit. A total of 15 levels can be produced by using S1, S2, S3, and S4 of level generation unit along with T1 and T2 of Polarity generation unit. By switching OFF S1, S2, S3, and S4 we can obtain zero level. Negative half cycle will be in symmetry with positive cycle, hence it can be generated by using S1, S2, S3, and S4 of level generation unit along with T2 and T3 of polarity generation unit.

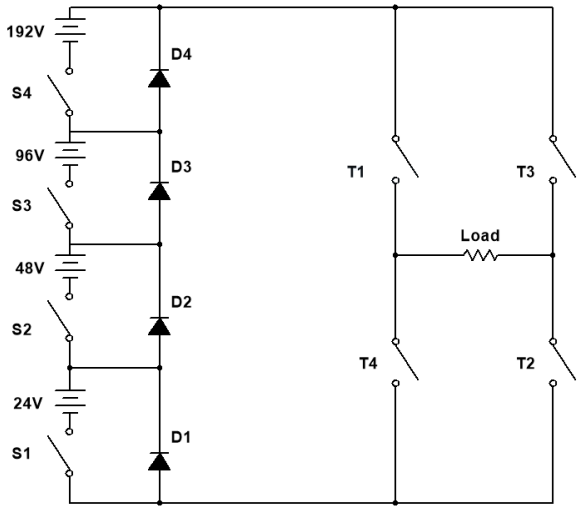

Fig. 3. Circuit Diagram

For example at state 3, Switches S1 and S2 are ON and diode D3 and D4 are forward biased. During positive half cycle we get Vo = V1 + V2. This is repeated for all other states to get output voltage values.

TABLE I. ON SWITCHES LOOK-UP TABLE

State	Switches States				Output Voltage
	S4	*S3*	*S2*	*S1*	
0	0	0	0	0	0
1	0	0	0	1	V_1
2	0	0	1	0	V_2
3	0	0	1	1	V_1+V_2
4	0	1	0	0	V_3
5	0	1	0	1	V_1+V_3
6	0	1	1	0	V_2+V_3
7	0	1	1	1	$V_1+V_2+V_3$
8	1	0	0	0	V_4
9	1	0	0	1	V_1+V_4
10	1	0	1	0	V_2+V_4
11	1	0	1	1	$V_1+V_2+V_4$
12	1	1	0	0	V_3+V_4
13	1	1	0	1	$V_1+V_3+V_4$
14	1	1	1	0	$V_2+V_3+V_4$
15	1	1	1	1	$V_1+V_2+V_3+V_4$

III. WORKING

From the above mentioned topology, it can be inferred that the voltage blocking capability of semiconductor devices, used in polarity generation unit is 'Vm'. Due to this, MOSFETs having high ratings will be used in the level generation part compared to polarity generation unit [17]. Trinary configuration utilizes a unique configuration where we can obtain different levels even by subtracting voltage levels.

Merits of this circuit are:

- Circuit is simple and modular
- Only unidirectional switches are used
- High rated switches can operate at fundamental frequency.

In open-loop operation, a fixed reference is taken which is not dependent on any measurement [18]. This reference is predetermined (Off-line calculations) for a particular operating point. This makes the dynamic response of the system poor. Requirement of Isolated DC sources and non-usability of trinary configurations are the limitations of this topology. Main aim of multilevel inverter is to increase the quality of harmonic contents which is represented by THD [11].

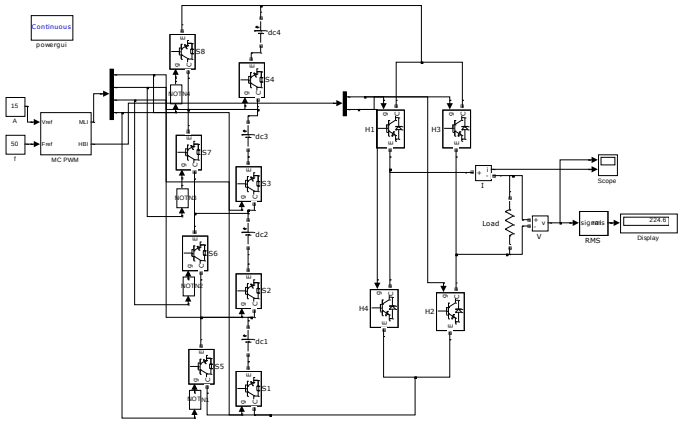

Fig. 4. Simulation diagram of the 31-level inverter

IV. SIMULATION RESULTS

The analysis of the result of 31-level inverter with optimal number of switches is shown below. The input voltage sources used are as follows, V1 =24V, V2 = 48V, V3 = 96V, V4 = 192V. Frequency of 50Hz is assumed for output voltage. Switching table shown in Table 1 gives the magnitude of the output voltage Vo for various states of the switches. Pulse generator output is given to the semiconductor switching device i.e. MOSFET.

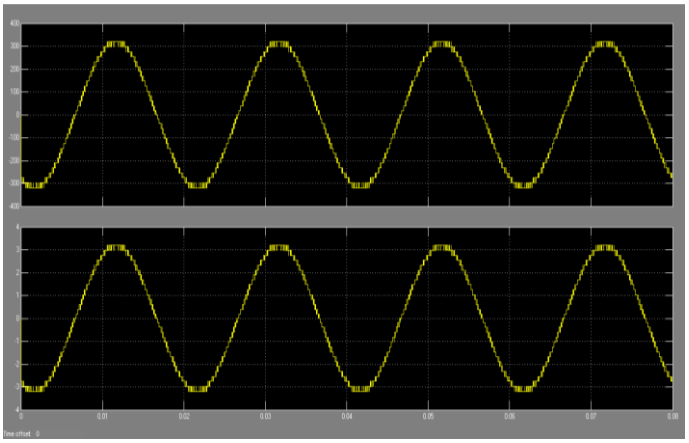

Fig. 5. Simulated output voltage and current waveforms

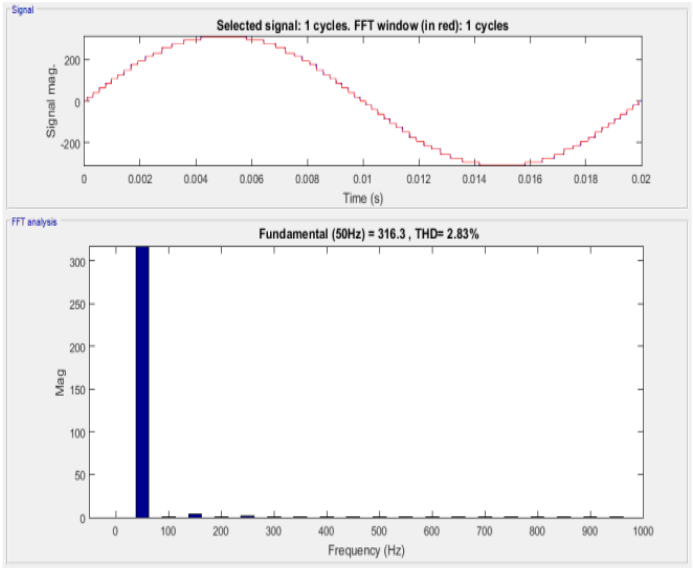

Fig. 6. Simulated output voltage waveform and Harmonic spectrum

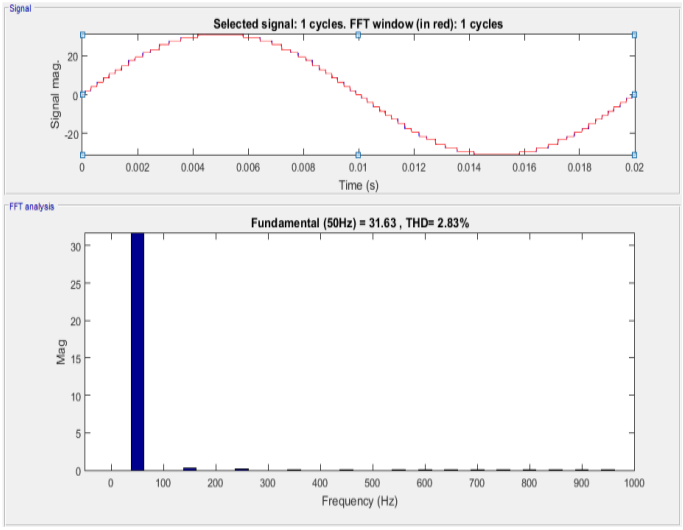

Fig. 7. Simulated output current waveform and Harmonic spectrum

These pulses have amplitude of 1V. The switch with highest stress operates at lowest frequency [19]. Load current and inverter output voltage are within the range of IEEE standard for harmonics (IEEE 519) i.e. 2.83%. This is shown in Fig. 6 and Fig. 7.

V. CONCLUSION

In this paper, an optimized multilevel inverter design for medium voltage systems is proposed. The primary advantage of this design is the simple structure which facilitates reduction in the size of the multilevel inverter and the complexity of the driving circuit. Simulation is performed using MATLAB/SIMULINK platform. A 31-level output with THD of 2.83% is obtained. Further, the features of this topology for higher output levels can be inferred from the results. A comparison of the various factors has been carried out for the recommended asymmetric topology versus other topologies. It can be seen that the blocking voltage values of the semiconductor switching devices in the MLDCL asymmetric structure inverter is lesser compared to other topologies which uses asymmetric structures. The simulated result for the proposed methods is presented here. It is proved that inverter with the presented topology needs lesser number of MOSFETs. By using this topology

we can equivalently reduce number of gate drivers, consequently reducing the size of the circuit. Addition of passive filters can hence be avoided resulting in energy efficiency.

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