Journal of Science and Technology
ISSN: 2456-5660 Volume 7, Issue 02 (MAR-APR 2022)

www.jst.org.in *DOI: https://doi.org/10.46243/jst.2022.v7.i02.pp42-53*

A Closed Loop Control Method for Renewable Energy Applications Using a New Hybrid Boosting Converter

Karri Sai Satyanath[1], Bathania Venkata Mohan[1], Kolluru Prasanth Kumar[1], Vendrapati Rakesh Kumar[1], Gampa Venkata Sai Lokesh[1], Chenna Rakesh Rao[1], I Prasanna Kumar[2] , Dr.N Samba Siva Rao[3]

[1]Department of Electrical and Electronics Engineering, NRI Institute of Technology, Agiripalli, India.
[2]Associate Professor, Department of Electrical and Electronics Engineering, NRI Institute of Technology, Agiripalli, India.
[3]Professor & Head, Department of Electrical and Electronics Engineering, NRI Institute of Technology, Agiripalli, India.

To Cite this Article

Karri Sai Satyanath, Bathania Venkata Mohan, Kolluru Prasanth Kumar, Vendrapati Rakesh Kumar, Gampa Venkata Sai Lokesh, Chenna Rakesh Rao, I Prasanna Kumar , Dr.N Samba Siva Rao*, "***A Closed Loop Control Method for Renewable Energy Applications Using a New Hybrid Boosting Converter***", Journal of Science and Technology, Vol. 07, Issue 02, March-April 2022.*

***Abstract*— Conventional sources like fossil fuels were used earlier to satisfy the energy demands. Nowadays these are being replaced by renewable sources like photovoltaic sources. In this paper, a hybrid boosting converter using photovoltaic system with closed loop Control is analyzed and simulated. A new hybrid boosting converter is used to increase the input dc voltage. In Existing method hybrid boosting converter used with one switch in the converter and produce pulses for that switch in open loop. By using the open loop method we get only output as produced amount of input which is given. Then we propose a closed loop method for HBC. By using this closed loop control technique we achieve required output voltage.**

Keywords*— Bipolar voltage multiplier (BVM), hybrid boosting converter (HBC), nature interleaving, renewable energy, single switch single inductor, Induction motor drive.

I. INTRODUCTION

As of late, the brisk change of sustainable power source system calls for new generation of high gain dc/dc converters with high productivity and minimal effort. The front end of "attachment and Play" PV system normally asks for wander up converter which is fit for boosting the voltage from 35 to 380Vwith control ability because of the low terminal voltage and the essential of MPPT following limit with respect to single PV board .Considering a breeze develop with inward mediumvoltage dc (MVDC)- system, a MVDC converter prepared to help the voltage from 1– 6 to 15– 60 kV is required to associate the output of generator-facing rectifier to the MVDC line . Some other vitality stockpiling systems, for instance, power module filled system moreover require high-gain dc/dc converter because of their low voltage level at limit side. Remembering the ultimate objective to accomplish high voltage change extent with high capability, various high gain upgrade methodology were researched in the past distributions. Among them, switched capacitor structure, tapped/coupled inductorbased method, transformer-based strategy voltage multiplier structure or blends of them pulled in huge considerations. Each technology has its one of a kind favorable circumstances and confinements. The switched capacitor dc– dc converter can achieve high adequacy however has throbbing present and poor control limit. Introduction of thunderous switched capacitor converter can relieve the throbbing current however does not comprehend the control issue.

The tapped-inductor and transformer encourages gain boosting capacity however requires snubber circuit to handle leakage issue. The bend of above headways as a general rule outputs promising circuit incorporates however with over the top number of parts. In this paper, gain change development in light of alteration of standard help converter while keeping up single inductor and single switch is analyzed, centering at enhancing the circuit configuration, diminishing the cost, satisfying the solicitations of common high gain applications, what's all the more, reassuring expansive scale fabricating. Gain upgrade from a help converter started from quadratic support. It accomplished higher voltage gain with a lone switch, yet exhibited high section voltage stretch. Regardless, this converter influenced high gain converter headway take after on.

Many gain development procedures for help converter by including just diodes and capacitors were inspected already. The procedure for uniting support converter with standard Dickson multiplier what's more, Cockcroft–Walton multiplier to make new topologies were proposed, for instance, topologies in Fig. 1(a) what's more, (b). Air center inductor or stray inductor was used inside voltage multiplier unit to diminish current throb. A fundamental circuit using the super lift procedure was proposed and stretched out to higher gain applications such as Fig. 1(c). Its accomplice of negative output topology and twofold outputs topology were proposed and analyzed furthermore. The possibility of multilevel help converters was researched
in and the topology of Fig. 1(d) was given as central source affiliation converter. Additionally, two switched capacitor cells were proposed and different topologies were dictated by applying them to the basic PWM dc– dc converters. Conventional topologies are showed up as Fig. 1(e) and (f). A changed voltage-lift cell was proposed and the topology of Fig. 1(g) was made. Propelled by the above topologies, another blend boosting converter (HBC) with single switch and single inductor is proposed by using bipolar voltage multiplier (BVM) in this paper.

The second-arrangement HBC is showed up as Fig. 1(h). Taken a gander at with other recorded topologies in Fig. 1, the proposed converter diminishes the voltage rating of output channel capacitor and showcases the nature interleaving operation properties. Differentiated and the converter in Fig. 1(d), the proposed converter has tinier

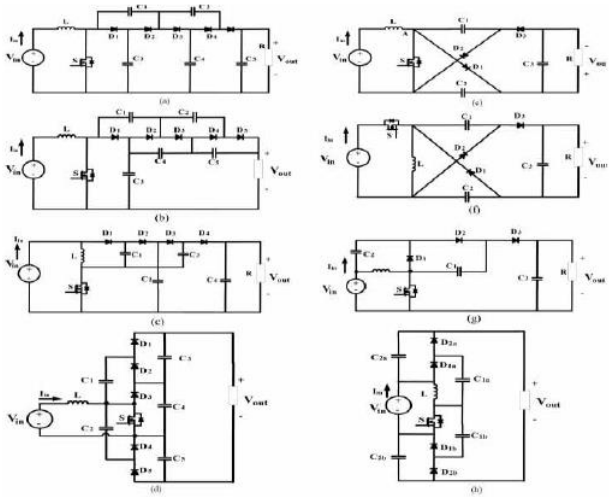


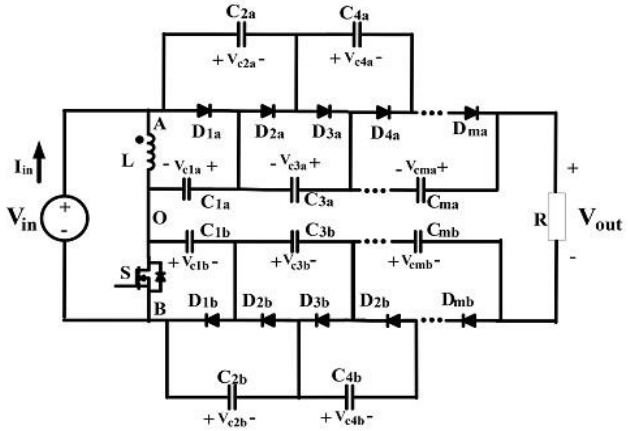
Figure 1. Previous high-gain dc–dc converters with single-switch single-inductor and proposed topology. (a) Boost + Dickson multiplier , (b) Boost + Cockcroft– Walton multiplier , (c) super lift with elementary circuit , (d) central source multilevel boost converter, (e) Cuk derived, (f) Zeta derived , (g) modified voltage lifter, and (h) proposed second-order HBC.

Output ripple and higher parts use rate as for change ratio. Some interleaving progresses for swell decline and power improvement were represented in the composition; however these systems are commonly in perspective of circuit branch advancement which requires more parts. The proposed topology has accomplished humbler swell with single switch what's more, single inductor while keeping up high voltage gain.

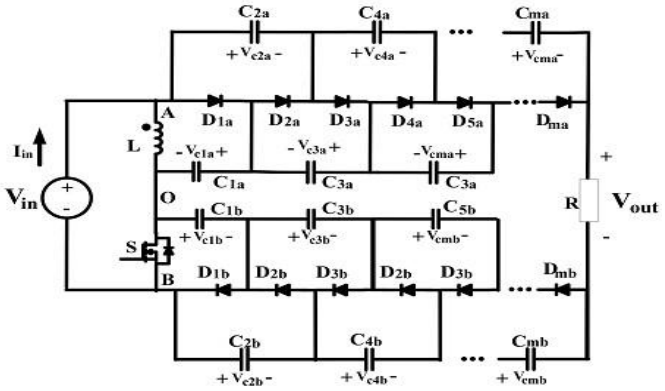
As of late, numerous more structures accomplishing higher gain were additionally reported, yet they embraced no less than two inductors on the other hand switches, or some depend on tapped inductor/transformer, which may confound the circuit design and increment cost.

II. PROPOSED GENERAL HBC TOPOLOGY AND ITS OPERATIONAL PRINCIPAL

The proposed HBC is shown in Fig. 3.2. There are two versions of HBC, odd order HBC and even-order HBC as shown in Fig. 3.2(a) and (b). The even-order topology integrates the input source as part of the output voltage, leading to a higher components utilization rate with respect to the same voltage gain. However, they share similar other characteristics andcircuit analysis method. Therefore, only even-order topology is investigated in this paper.



(a)



(b)

Fig.3.2. Proposed general HBC topology. (a) Odd-order HBC. (b) Even-order HBC.

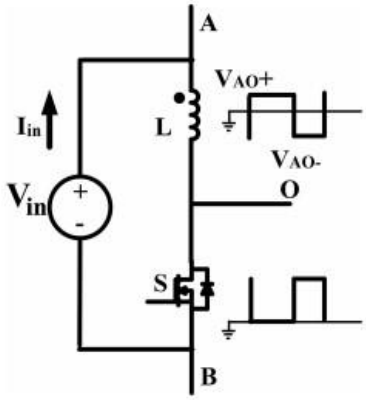


Fig.3.3. Inductive three-terminal switching core

A. Inductive Switching Core

In a HBC topology, the inductor, switch and input source serve as an "inductive switching core," shown as Fig. 3.3. It can generate two "complimentary" PWM voltage waveforms at port AO and port OB. Although the two voltage waveforms have their individual high voltage level and low voltage level, the gap between two levels is identical, which is an important characteristic of inductive switching core for interleaving operation.

B. BVM

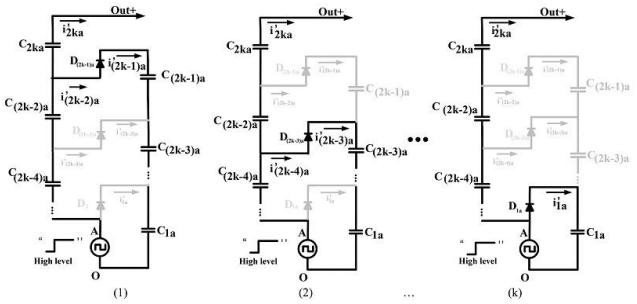
A BVM is composed of a positive multiplier branch and a negative multiplier branch, shown in Fig. 3.4(a) and (b). Positive multiplier is the same as traditional voltage multiplier while the negative multiplier has the input at the cathode terminal of cascaded diodes, which can generate negative voltage at anode terminal, shown in Fig.3.4 (b). By defining the high voltage level at input AO as VOA+, the low voltage level as VOA−, and the duty cycle of high voltage level as D, the operational states of the even-order positive multiplier is derived as Fig. 5 and illustrated as following:

State 1[0, DTs]: When the voltage at port AO is at high level, diodes Dia (i=2k−1, 2k−3...3, 1) will be conducted consecutively. Each diode becomes reversely biased before the next diode fully conducts. There are K sub states resulted as shown in Fig. 3.4(a). Capacitor Cia (i=2, 4...2k) are discharged during this time interval. Assuming the flying capacitors get fully charged at steady state and diodes voltage drop are neglected, the following relationship can be derived:

$$V_{c1a} = V_{\mathrm{AO+}} \tag{3.1}$$

$$V_{\mathrm{cia}} = V_{c(i+1)a}(i = 2,4,6,\ldots,2k-2) \tag{3.2}$$

State 2[dTs, Ts]: When the voltage at port AO steps to low level, diode D2ka is conducted first, shown as Fig.3.4 (b)-(1). Then the diodes Dia (i=2, 4, ... 2k−2) will be turned on one after another from high number to low. Each diode will be turned on when the previous one becomes blocked. Only diode D2ka is conducted for the whole time interval of [0, dTs], since capacitor C (2k−1) a has to partially provide the



(a)

Fig.3.4. Operation modes of even-order BVM positive branch. (a) State 1[0, DTs]. (b) State 2[DTs, Ts]

Load current during the whole time interval. Even though not all the diodes are conducted and blocked at the same time, the flying capacitors still have the following relationship by the end of this time interval: $V_{c2a} = V_{c1a} - V_{\mathrm{AO-}}$ $V_{\mathrm{cia}} = V_{c(i+1)a}(i = 3,5,7,\ldots,2k-1)$

According to charge balance principal, the total amount of electrical charge flowing into capacitors Cia (i=2, 4 ... 2k) should equal to that coming out from them in a switching period at steady state, therefore

$$\sum_{i=1}^{k} \int_{0}^{\mathrm{DT}_S} i'_{2ia}\,dt = \sum_{i=1}^{k} \int_{DT_S}^{T_S} i_{2ia}\,dt \tag{3.5}$$

Thus, the capacitor group Cia (i=2, 4...2k) can be replaced by an equivalent capacitor C2a (eq). The diode group Dia (i=2, 4...2k) which provides the charging path for C2a (eq) is equivalent to a single diode C2a (eq). Similarly,

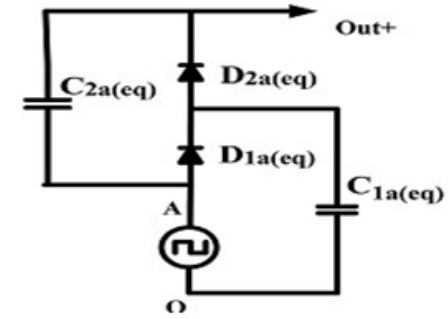
the capacitor group Cia (i=1,3, ... 2k−1) can be replaced by an equivalent capacitor C1a (eq) and diode group Dia (i= 1,3, ... 2k−1) by D1a (eq) . The final equivalent even-order positive multiplier branch is given as Fig.3.5 (a). A similar analysis yields the equivalent negative multiplier branch as shown in Fig.3.5 (b). According to (1)–(4), the voltage of equivalent capacitors C1a (eq), C2a (eq) can be expressed as following:

$$V_{c2a(eq)} = k(V_{AO+} - V_{AO-}) \tag{3.6}$$

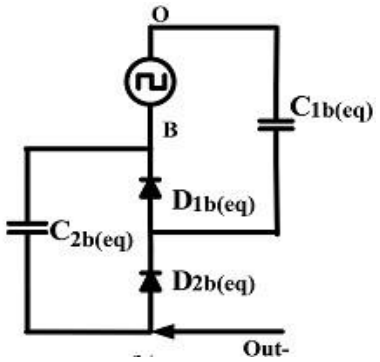
$$V_{c1a(eq)} = (k-1)(V_{AO+} - V_{AO-}) + V_{AO+} \tag{3.7}$$

For the negative branch shown in Fig.3.5 (b), the following results can be obtained based on similar analysis:

$$V_{c2b(eq)} = k(V_{OB+} - V_{OB-})$$



(a)



(b)

Fig.3.5. Equivalent circuit. (a) Even-order positive multiplier. (b) Even-order negative multiplier

Where $V_{OB}+$ is the high voltage level of input port OB and $V_{OB}-$ is the low voltage level. 3) Equivalent Capacitance Derivation: Assuming capacitors Cia (i=1, 2, 3, ... 2k) have the same capacitance C, in order to derive the equivalent capacitance of C2a (eq) and C1a (eq) in expression of C, a voltage ripple-based calculation method is proposed in this section. Assuming the peak to peak voltage ripple of the flying capacitors can be expressed as ΔVcia (i=1, 2, 3...2k), the ripple of equivalent capacitor C2a (eq) is ΔV, the following relationship can be approximated:

$$\boxed{\Delta V = \Delta V_{c2a} + \Delta V_{c4a} + \dots \Delta V_{c2ka}} \tag{3.10}$$

$$\boxed{\overline{i'_{ia(\text{on})}} DT_S = \overline{i_{ia(\text{off})}} D'T_S (i = 2, 4, \dots 2k)} \tag{3.11}$$

Based on the (3.11)–(3.13), the following relationship can be obtained:

$$\overline{i_{2a(\text{off})}} = \overline{i_{4a(\text{off})}} = \dots \overline{i_{(2k-4)a(\text{off})}} = \overline{i_{(2k-2)a(\text{off})}} = \overline{i_{(2k-1)a(\text{off})}} \tag{3.14}$$

Based on charge balance of capacitor C2ka, it can be derived that

$$\overline{i_{2(k-1)a(\text{off})}}D'T_S = I_O T_S \tag{3.15}$$

$$\overline{i_{2ka(\text{off})}}D'T_S = \overline{i'_{2ka(\text{on})}}DT_S = I_o DT_S \tag{3.16}$$

Where

$I_o = \frac{V_{\text{out}}}{R}$.

According to KCL in Fig. 3.4(b), voltage ripple of capacitors Cia (i=2, 4...2k) can be obtained

$$\begin{cases} C\Delta V_{c2a} = (\overline{i_{2ka(\text{off})}} + \overline{i_{2k-2a(\text{off})}} + \dots \overline{i_{4a(\text{off})}} \\ \qquad + \overline{i_{2a(\text{off})}})D'T_S \\ C\Delta V_{c4a} = (\overline{i_{2ka(\text{off})}} + \overline{i_{2k-2a(\text{off})}} + \dots \overline{i_{4a(\text{off})}})D'T_S \\ \qquad \dots \\ C\Delta V_{c2ka} = \overline{i_{2ka(\text{off})}}D'T_S \end{cases}$$

Where

$D' = 1 - D$

Based on the equations from (3.14) to (3.16), the equation group (3.17) can be reduced to the following expression:

$$\begin{cases} C\Delta V_{c2a} = (k - 1 + D)I_O T_S \\ C\Delta V_{c4a} = (k - 2 + D)I_O T_S \\ \dots \\ C\Delta V_{c2ka} = (0 + D)I_O T_S \end{cases} \tag{3.18}$$

Substituting (3.10) to (3.18), the following equation is derived:

$$C\Delta V = \left(\frac{k(k-1)}{2} + kD\right) I_O T_S \tag{3.19}$$

Meanwhile, the following equation can be derived based on discharging stage of equivalent capacitor C2a (eq)

$$C_{2a(eq)}\Delta V = I_O DT_S \tag{3.20}$$

Based on (3.19) and (3.20), the equivalent capacitor C2a (eq) can be expressed

$$C_{2a(eq)} = \frac{2D}{k(k-1+2D)}C \tag{3.21}$$

Similarly, in order to derive the equivalent capacitance of C1a (eq), the following equation can be derived:

$$\begin{cases} C\Delta V_{c1a} = kI_O T_S \\ C\Delta V_{c3a} = (k-1)I_O T_S \\ \qquad \dots \\ C\Delta V_{c2(k-1)a} = I_O T_S \end{cases} \tag{3.22}$$

At the same time, the following equation exists:

$$C_{1a(eq)}\Delta V' = I_O T_S \tag{3.23}$$

Where

$\Delta V' = \Delta V_{c1a} + \Delta V_{c3a} + \dots \Delta V_{c(2k-1)a}$.

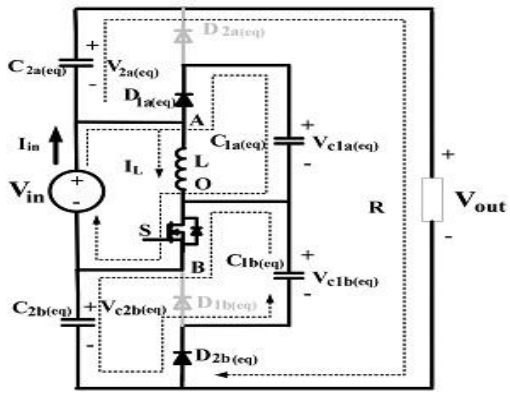
Therefore, the expression of C1a (eq) is obtained

$$C_{1a(eq)} = \frac{2}{(k+1)k}C \tag{3.24}$$

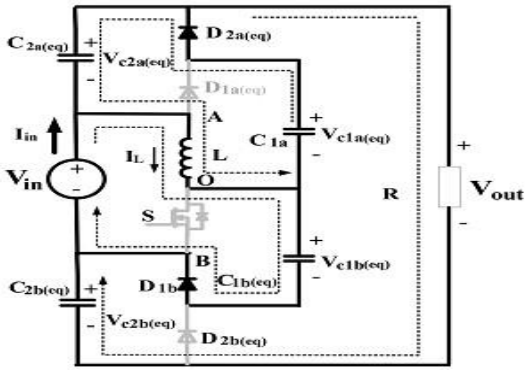
$$C_{1b(eq)} = \frac{2}{(k+1)k}C$$

$$C_{2b(eq)} = \frac{2D'}{k(k-1+2D')}C$$

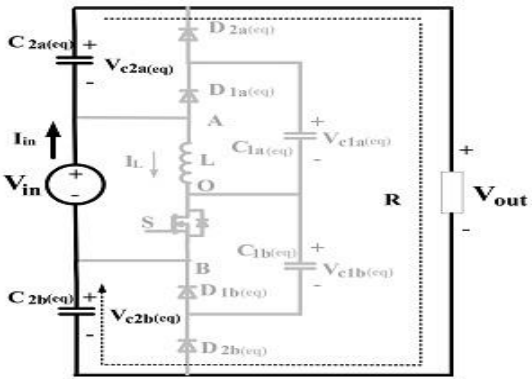
Because of the symmetry, the equivalent capacitance C1b (eq) and Cb (eq) is given as following



(a)



(b)



(c)

Fig.3.6. Three operation states. (a) State 1[0, DTs]. (b) State 2[DTs, (D+D1)Ts]. (c) State 3[(D+D1) Ts, Ts]

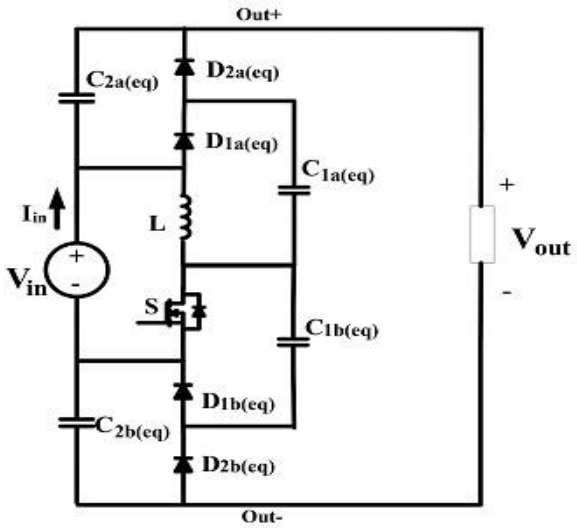


Fig.3.7. Equivalent even-order HBC

The derivation of voltage and equivalent value of the equivalent flying capacitors can facilitate the output voltage calculation and ripple estimation.

III. MATLAB/SIMULINK RESULTS

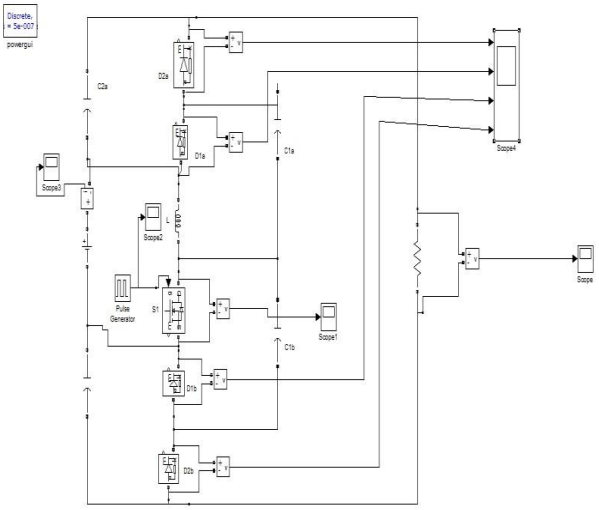
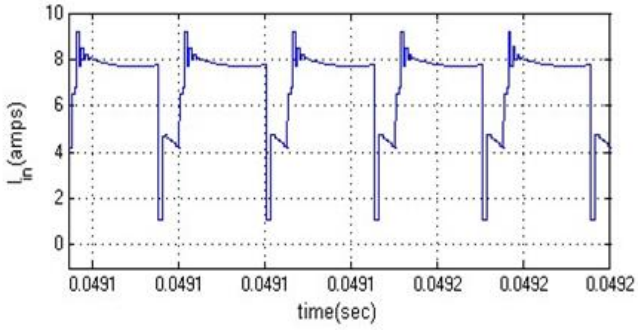


Fig.4.3 MATLAB/SIMULINK circuit for hydbrid boost converter



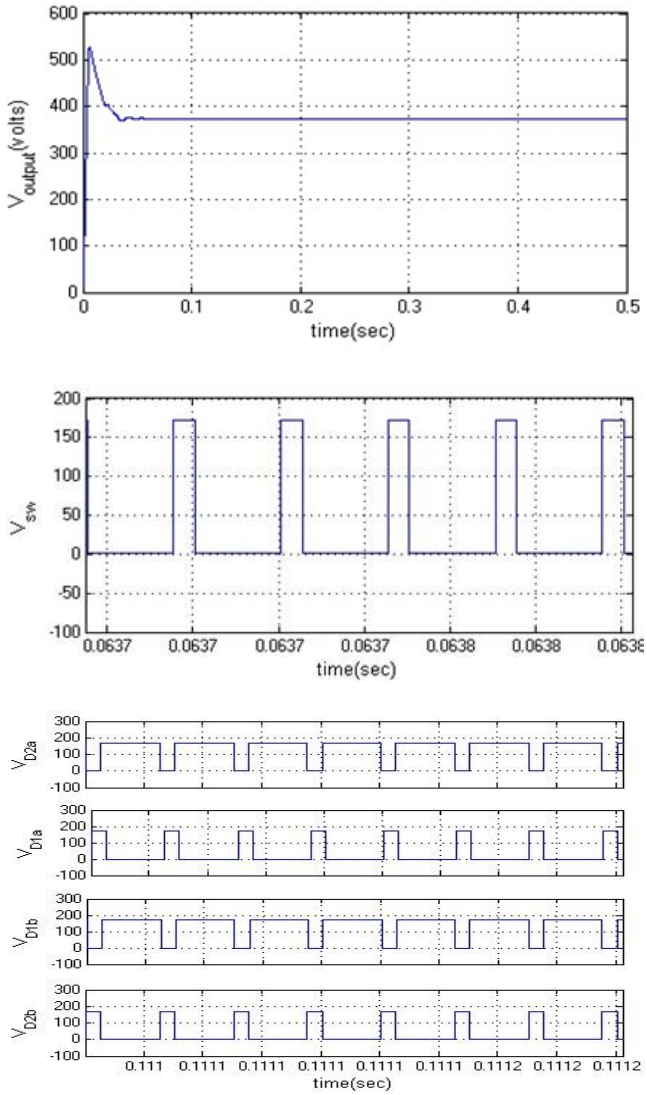


Fig.4.4 Experimental waveforms. (a)Vds, Iin, Vout, Vin. (b) Diodes voltage: Vd2a, Vd1a, Vd1b, Vd2b.

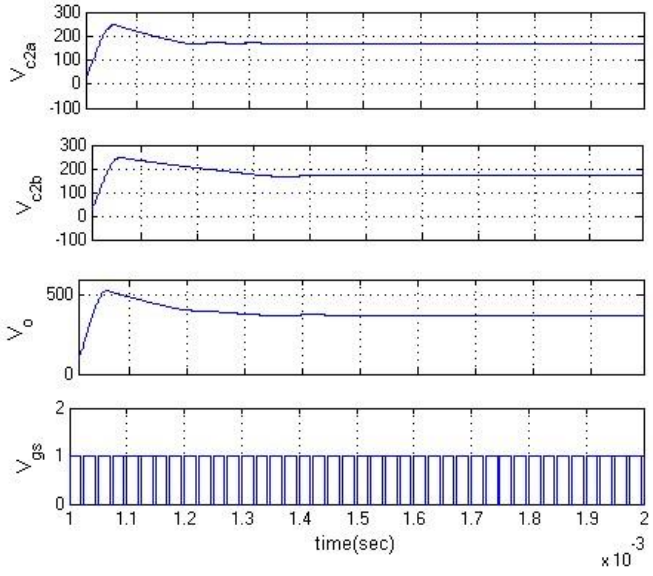


Fig.4.5 Experimental waveforms of voltage ripples: Vc2a, Vc2b, Vout and driving signal Vgs under (a) D=0.5

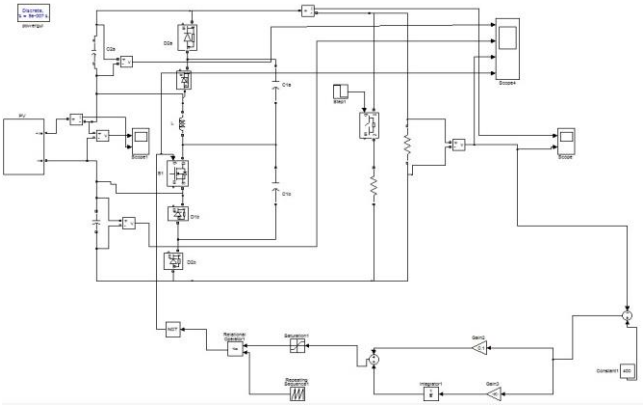


Fig.4.6 MATLAB/SIMULINK circuit for closed loop control of hybrid boost converter with PV system

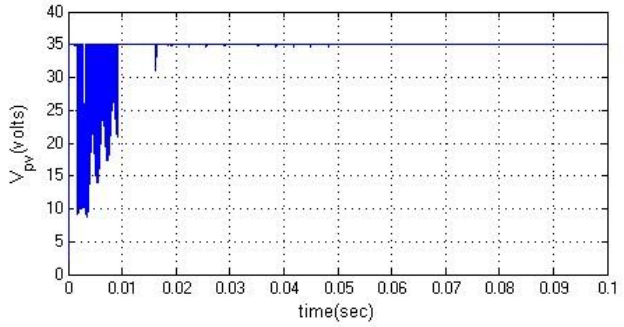


Fig.4.7 PV Voltage (V)

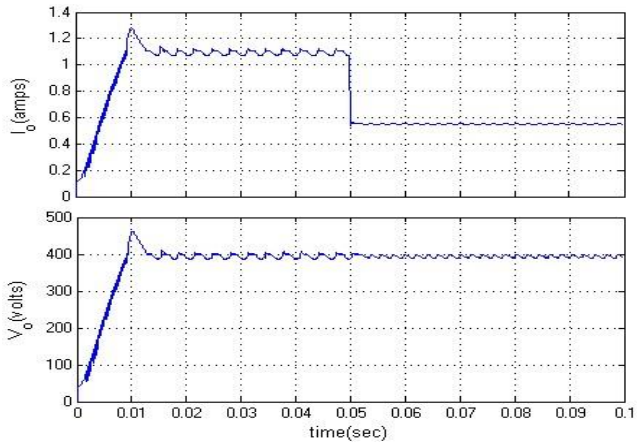


Fig.4.8 Outputs of Voltage and Current Sudden Decrease in Load:

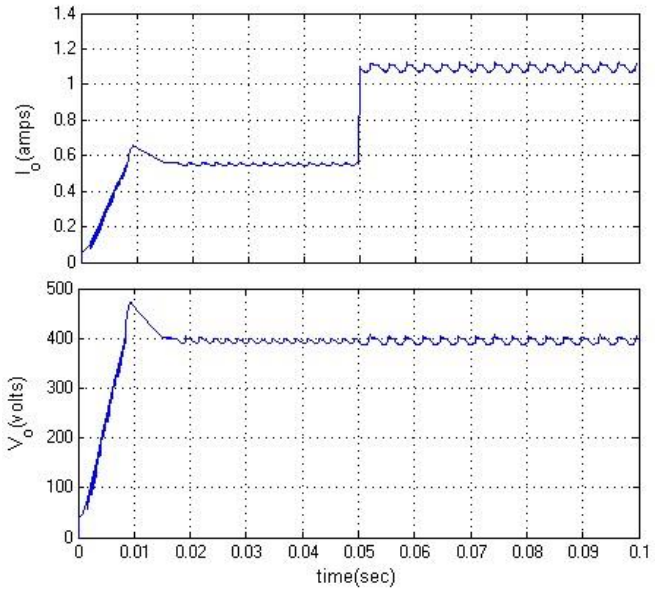


Fig.4.9 Outputs of Voltage and Current

IV. CONCLUSION

This paper exhibits another HBC utilized here for boosting the input low voltage to high level voltage. In this project we needs required sum or high voltage so we go for close circle or input method by utilizing criticism method we take output voltage as criticism and contrast that voltage and reference voltage or required voltage and provide for PI controller and we tuned the blunder and delivers pulses for switch which is utilized as a part of hybrid boost converter. These pulses for switch utilized as a part of the converter changes as indicated by what measure of output voltage creates yet in proposed method we get just a single output and change that output due to there is no criticism yet in expansion method we utilize input we get required measure of voltage until the point when the input give flags and pulses are change as per these signs we get output.

V. REFERENCES

[1] W. Chen, A. Q. Huang, C. Li, G. Wang, and W. Gu, "Analysis and comparison of medium voltage high power DC/DC converters for offshore wind energy systems,"IEEE Trans. Power Electron., vol. 28, no. 4, pp. 2014–2023, Apr. 2013.

[2] J. A. Starzyk, "A DC-DC charge pump design based on voltage doublers," IEEE Trans. Circuits Syst. I Fundam. Theory Appl., vol. 48, no. 3, pp. 350–359, Mar. 2001.

[3] F. L. Luo and H. Ye, "Positive output multiple-lift push–pull switched capacitor luoconverters," IEEE Trans. Ind. Electron., vol. 51, no. 3, pp. 594–602, Jun. 2004.

[4] N. Vazquez, L. Estrada, C. Hernandez, and E. Rodriguez, "The tapped inductor boost converter," in Proc. IEEE Int. Symp. Ind. Electron., Jun. 2007, pp. 538–543.

[5] R. Wai, C. Lin, R. Duan, and Y. Chang, "High-efficiency DC-DC converter with high voltage gain and reduced switch stress," IEEE Trans. Ind. Electron., vol. 54, no. 1, pp. 354–364, Feb. 2007.

[6] J. Lee, T. Liang, and J. Chen, "Isolated coupled-inductor-integrated DC–DC converter with non dissipative snubber for solar energy applications," IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3337–3348, Jul. 2014.

[7] M. Delshad and H. Farzanehfard, "High step-up zero-voltage switching current-fed isolated pulse width modulation DC–DC converter," IET Power Electron., vol. 4, no. 3, pp. 316–322, Mar. 2011.

[8] A. Lamantia, P. G. Maranesi, and L. Radrizzani, "Small-signal model of the Cockcroft-Walton voltage multiplier," IEEE Trans. Power Electron., vol. 9, no. 1, pp. 18–25, Jan. 1994.

[9] P. Lin and L. Chua, "Topological generation and analysis of voltage multiplier circuits," IEEE Trans. Circuits Syst., vol. 24, no. 10, pp. 517–530, Oct. 1977.

[10] K.-C. Tseng, C.-C. Huang, and W.-Y. Shih, "A high step-up converter with a voltage multiplier module for a photovoltaic system,"IEEE Trans. Power Electron., vol. 28, no. 6, pp. 3047–3057, Jun. 2013.

[11] W. Li, W. Li, X. Xiang, Y. Hu, and X. He, "High step-up interleaved converter with built-in transformer voltage multiplier cells for sustainable energy applications,"IEEE Trans. Power Electron., vol. 29, no. 6, pp. 2829–2836, Jun. 2014.

[12] X. Hu and C. Gong, "A high voltage gain DC–DC converter integrating coupledinductor and diode–capacitor techniques," IEEE Trans. Power Electron., vol. 29, no. 2, pp. 789–800, Feb. 2014.
[13] D. Cao and F. Z. Peng, "A family of zero current switching switched capacitor dc-dc converters," in Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo., Feb. 2010, pp. 1365–1372.
[14] J. Yao, A. Abramovitz, and K. Smedley, "Steep gain bi-directional converter with a regenerative snubber," IEEE Trans. Power Electron., vol. 8993, no. c, p. 1, 2015.
[15] D. Maksimovic and S. Cuk, "Switching converters with wide DC conversion range," IEEE Trans. Power Electron., vol. 6, no. 1, pp. 151–157, Jan. 1991.
[16] B. Axelrod, G. Golan, Y. Berkovich, and A. Shenkman, "Diode–capacitor voltage multipliers combined with boost-converters: Topologies and characteristics," IET Power Electron., vol. 5, no. 6, pp. 873–884, Jul. 2012.
[17] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage multiplier cells applied to converters, non-isolated DC–DC,"IEEE Trans. Power Electron., vol. 23, no. 2, pp. 871–887, Mar. 2008.
[18] F. L. Luo, S. Member, and H. Ye, "Positive output super-lift converters," IEEE Trans. Power Electron., vol. 18, no. 1, pp. 105–113, Jan. 2003.
[19] F. L. Luo and H. Ye, "Negative output super-lift converters," IEEE Trans. Power Electron., vol. 18, no. 5, pp. 1113–1121, Sep. 2003.
[20] F. L. Luo, "Double output Luo-converters-voltage lift technique," in Proc. Int. Conf. Power Electron. Drives Energy Syst. Ind. Growth, 1998, pp. 342–347.