

A Comprehensive Analysis of 32nm technology of Ladner Fischer Adder using CMOS Logic, PTL, and DPTL Focusing on Power

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ABSTRACT

Adders are designed as essential components in digital signal processing and VLSI technologies. Among them, parallel prefix adders offer significant speed advantages over traditional binary adders for various electronic applications. This paper explores the design of a 4-bit Ladner Fischer Adder using different technologies like CMOS, Pass Transistor Logic, and Double Pass Transistor Logic to achieve a more efficient use of low power. These implementation results demonstrate that the Ladner Fischer adder designed with CMOS, PTL, and DPTL has reduced power consumption. The simulation was performed using Dsch3 and micro wind 3.1 tool.

KEYWORDS: Large-scale integration, Ladner Fischer adder, parallel prefix adder Complementary Metal Oxide Semiconductor, Pass Transistor Logic, Double Pass Transistor Logic.

I. INTRODUCTION

The computation operations of binary numbers are one of the most stimulating problems in ultramodern digital systems causing major design trouble for digital signal processors and general-purpose microprocessors. The design of high-speed, low-power, and area-effective double adders always receives a great deal of attention. Surrounded by the hundreds of adder infrastructures known in the literature, when high performances are obligatory, parallel prefix trees are generally preferable. Parallel prefix Adders have been honored as the most effective circuits for binary addition in digital systems. Their regular structure and fast performance make them substantially seductive for VLSI perpetration. The need for parallel Prefix adders is that it's primarily presto when compared with ripple carry adders. Parallel Prefix adders have been honored as the most effective circuits for binary addition. This paper investigates the performance of Ladner Fischer Adder. Ladner Fischer's parallel prefix adder is brisk and uses lower power than

BrentKung's and Kogge Stone's. The Ladner-Fischer parallel prefix adder consumes significantly lower power than other types of adder

PARALLEL PREFIX ADDERS

Parallel prefix adder is a kind of adder that uses prefixoperation to do efficient addition A parallel prefix adder is a type of digital circuit used to efficiently compute the sum of multiple binary numbers in parallel. This results in faster addition of large numbers with reduced hardware complexity.

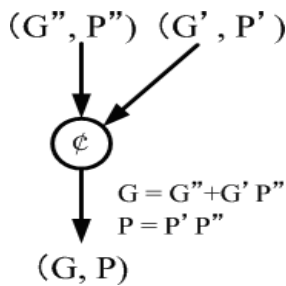


Figure 1. Carry operator

Parallel prefix adders are constructed out of fundamental carry operators denoted by ϕ as follows: $(G'', P'') \phi (G', P') = (G'' + G' P'', P' P'')$ where P'' and P' indicate the carry propagations, G'' and G' indicate the carry generations. Where P'' and P' indicate the carry propagations, G'' and G' indicate the carry generations.

CMOS (complementary metal oxide semiconductor)

CMOS stands for Complementary Metal-Oxide-Semiconductor, which is a technology used in the fabrication of integrated circuits (ICs). It involves the use of both p-type and n-type metal-oxide-semiconductor field-effect transistors (MOSFETs) to achieve low power consumption and high noise immunity. CMOS technology is widely used in digital ICs, such as microprocessors, memory chips, and other digital logic circuits, due to its low power consumption, high packing density, and relatively low manufacturing cost. By using this CMOS technology, we built the AND, XOR, and OR gates. We implement the CMOS Ladner Fischer adder by using AND, XOR, and OR gates. In the CMOS logic gates, for the NMOS transistor, whenever the gate to source voltage is less than the threshold voltage, then the MOSFET will act as an open switch. And whenever this voltage is more than the threshold voltage, then it will act as a closed switch.

Figure 2. CMOS AND gate

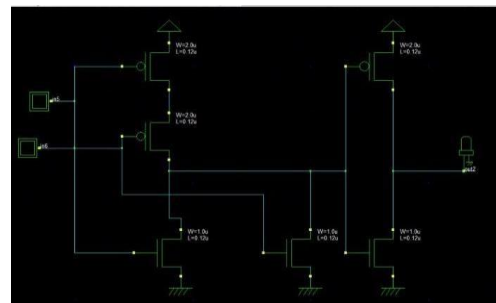
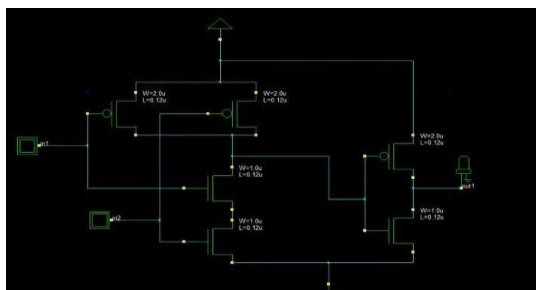


Figure 3. CMOS OR gate

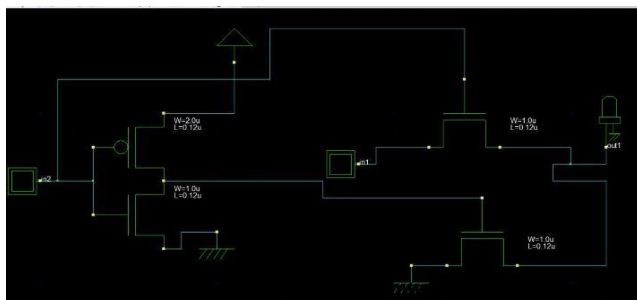
Here OR and AND logic gates proceed with NOR and NAND logic gates with inverter. The AND logic gate contributes when both of its inputs as given high (1) then output is high

(1). It is also intended by using NOT and NAND gates (NOT+NAND). The OR logic gate contributes when one of its Input is high (1) then output is also high (1). It is also intended to use NOT and NOR gates (NOT+NOR).

PASS TRANSISTOR LOGIC(PTL)

A marketable and broadly used alternative to complementary CMOS is Pass-Transistor Logic. In Pass Transistor Logic, the MOSFET is used as a switch. It reduces the no. of transistors used to make different logic gates, by destruction of redundant transistors. So whenever this MOS transistor is in the ON condition, then it passes the logic level from the input to the output side. And whenever these transistors are in the OFF condition, then it will isolate the input from the output side. So, in the CMOS logic gates, we have seen that, for the NMOS transistor, whenever the gate-to-source voltage is less than the threshold voltage, then the MOSFET will act as an open switch. And whenever this voltage is more than the threshold voltage, then it will act as a closed switch. Similarly, for the PMOS transistor, whenever this source-to-gate voltage is less than the threshold voltage, then the transistor will act as an open switch. And whenever this voltage is more than the threshold voltage, then it will act as a closed switch. So, in this way by using this MOS transistor as a switch, it is possible to transfer the logic level from the input to

the output side. Using this pass transistor logic, it is possible to build the different logic gates. By using PTL logic we implement the AND and OR gates.



The above figure represents an AND gate using PTL and it is designed by using two n-type MOSFET in series connection connected in Pass Transistor Logic proceed with NAND and NOT gates.

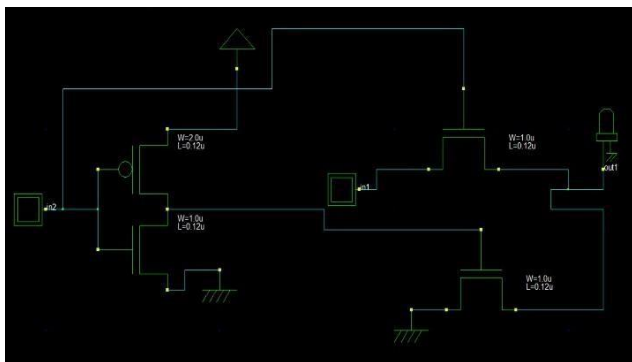


Figure 5. PTL OR gate

The OR gate is designed by using two n-type MOSFET parallel connection. Here Pass Transistor Logic there is no p-type of MOSFETs used in AND&OR logic gates design.

DOUBLE PASS TRANSISTOR LOGIC(DPTL)

Double pass transistor logic (DPTL) is a modified version of complementary pass transistor logic that meets the requirement of reduced supply voltage design. Achieving full swing operation in DPTL circuits is accomplished merely by introducing a PMOS transistor in parallel with the NMOS transistors. Its regular arrangement and double-transmission characteristics improve the gate speed without increasing the input capacitance. Has a simple design and has low contribution to static power. The structure of double-pass transistor logic is the solution to the problem of the complementary transistor logic which is the noise margin. Number of transistors and number of nodes is quite high.

Figure 6. DPTL OR gate

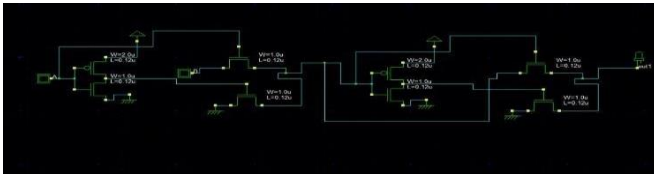


Figure 7. DPTL AND gate

By using DPTL logic we implement the AND & OR gates is designed. In this DPTL logic, we use both n-type and p-type MOSFETs and use the two-pass transistor and these are connected in series.

LADNER FISCHER ADDER

- The parallel prefix adders are utilized in numerous electronic applications due to their quick execution in number-crunching operations
- The operation of Parallel Prefix Adders is concluded in a Parallel manner.
- Here there's no prerequisite for Full adders. At that point, it gives less speed operation.
- The Parallel Prefix adder is outlined by utilizing Parallel Prefix Calculation which is considered as three stages.
- They are the Preprocessing stage, parallel prefix calculation stage, and computing entirety. This Parallel prefix adder gives proliferate P_i and produces G_i functions.
- Ladner-Fischer adder could be a structure that speeds up the method of expansion.
- Ladner-Fischer adder comprises the dark cell and gray cell. The dark cell comprises two AND gates and one OR gate. The gray cell comprises one AND & one OR entryway. The Ladner-Fischer adder comprises three stages. There are three stages in Ladner Fischer's adder.

1. pre-processing stage $P_i = ab' + a'b$ $G_i = a$ and carry generation
 stage $C_p = p1.p0$
 $C_g = g1 + p1.p0$

2. post-processing stage $S_i = p_i \text{ XOR } c_{i-1}$

3. using Ladner Fischer Adder. In CMOS logic several NMOS and PMOS transistors are used. Here the OR & AND gates are Proposed with NOR and NAND logic gates with inverters. The OR & AND logic gates using CMOS logic design are figured in Figure. 2 and Figure. 3

BLACK CELL

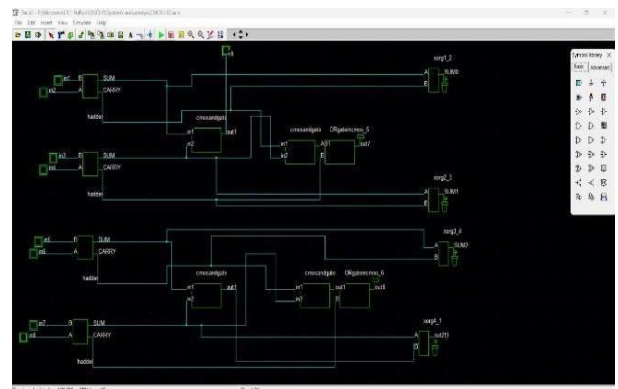
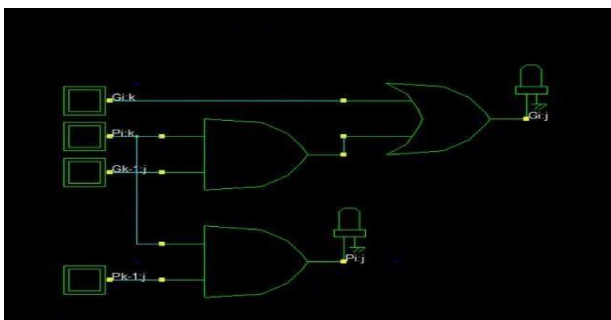
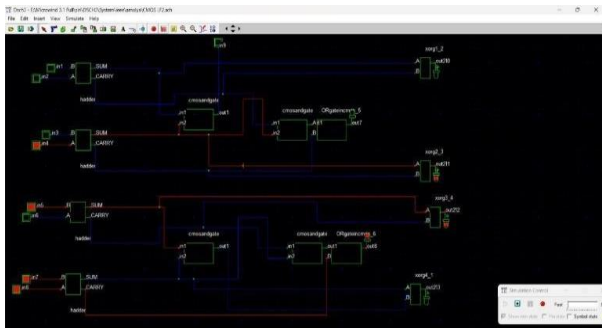


Figure 8. black cell

The Black cell consists of four inputs ($G_i: k$, $P_i: k$, $G_{k-1}: j$, $P_{k-1}: j$) and three logic gates- two AND and one OR gate.

The outputs $G_i: j$ and $P_i: j$ in the above diagram are given as inputs to the next Black cell along with $P_{k-2}: j$ and $G_{k-2}: j$. The process is repeated until the desired outputs are obtained. The black cell utilizes more memory and delay. Black cells can be replaced by Gray cells. Fischer Adder



GRAY CELL

Figure 8. Gray cell

The gray cell is a logical adder gate that contains only three inputs ($G_i: k$, $P_i: j$, $G_{k-1}: j$). The output from the Gray cell $G_i: j$ is given as input to the next Gray cell.

II. Methodology

DESIGN OF PROPOSED CMOS-BASED LADNER FISCHER ADDER

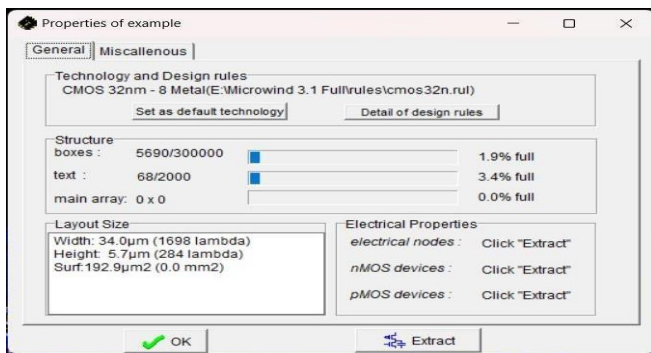
The 4-bit Ladner Fischer Adder is designed by using various logic gates such as XOR, AND, OR. By using these gates, we design the Black and Gray cells. Here the CMOS logic is applied to the AND & OR gates

Figure 10. execution results of CMOS-based 4-bit Ladner

Fischer Adder

To attain results from the design, let us consider the input bits 00, 01, 10, 11, and $C_{in}=0$. It gives the output sum = 0110 and carryout=1110. Microwind3.1 tool is used to obtain the Area and Power results of a 4-bit Ladner Fischer adder using CMOS logic. The Area results are shown in Figure 11.

Figure 11. Area results of CMOS-based parallel prefix Ladner Fischer Adder



If we observe the above figure, we conclude that the Area occupied by 4-bit using CMOS logic Ladner Fischer Adder is given as 192.9 μm^2 . The Power observed is 5.124uw from the design simulation.

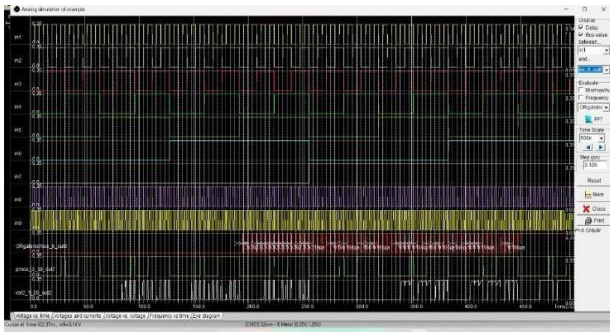


Figure 12. simulation results of CMOS-based 4-bitLadner Fischer Adder

DESIGN OF PROPOSED PTL-BASED LADNERFISCHER ADDER

The 4-bit Ladner Fischer Adder is designed by using various logic gates such as XOR, AND, OR. By using these gates, we design the black and gray cells. Here thePTL logic is applied to the AND&OR gates using Ladner Fischer Adder. In PTL logic several NMOS or PMOS transistors are used. Here the OR & AND gates are Proposed with NOR and NAND logic gates with inverters. The OR & AND logic gates using PTL logic design are figured in Figure. 4 and Figure. 5

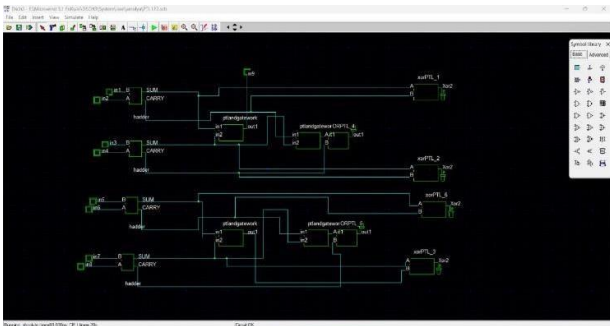


Figure 12. PTL-based Parallel prefix 4-bit Ladner FischerAdder

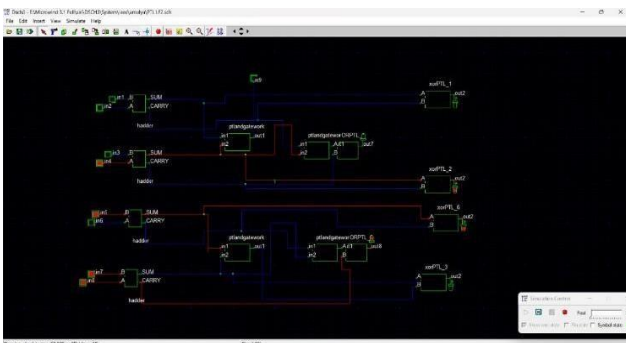


Figure13. execution results of ptl-based 4-bit Ladner Fischer Adder

To attain results from the design, let us consider the input bits 00, 01, 10, 11, and $C_{in}=0$. It gives the outputsum = 0110 and carryout=1110. Microwind3.1 tool is used to obtain the Area and Power results of the 4-bit Ladner Fischer adder using PTL logic. The Area resultsare shown in Figure 14.

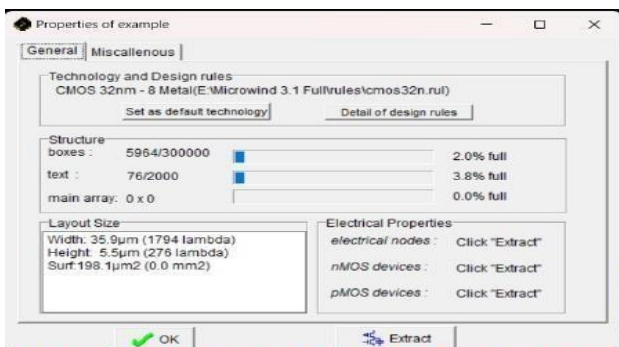


Figure 14. Area results of PTL-based parallel prefix 4-bit Ladner Fischer Adder

If we observe the above figure, we conclude that the Area occupied by 4-bit using PTL logic Ladner Fischer Adder is given as 198.9 μm^2 . The Power was observed as 3.925um from the design simulation.

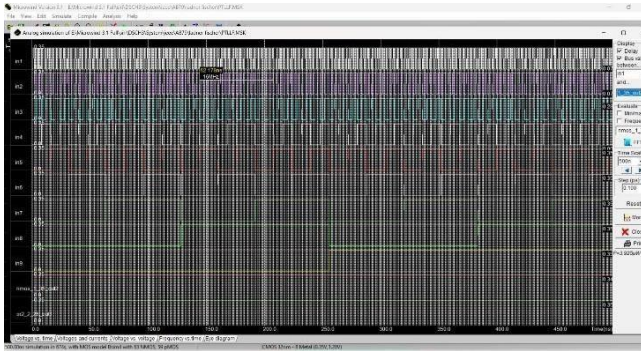


Figure 15. simulation results of PTL based 4-bit Ladner Fischer Adder

DESIGN OF PROPOSED DPTL-BASED LADNERFISCHER ADDER

The 4-bit Ladner Fischer Adder is designed by using various logic gates such as XOR, AND, OR. By using these gates, we design the black and gray cells. Here the DPTL logic is applied to the AND&OR gates using Ladner Fischer Adder. In DPTL logic several NMOS or PMOS transistors are used. Here the OR & AND gates are Proposed with NOR and NAND logic gates with inverters. The OR & AND logic gates using DPTL logic design are figured in Figure. 6 and Figure. 7

Figure 16. DPTL-based Parallel prefix Ladner Fischer Adder

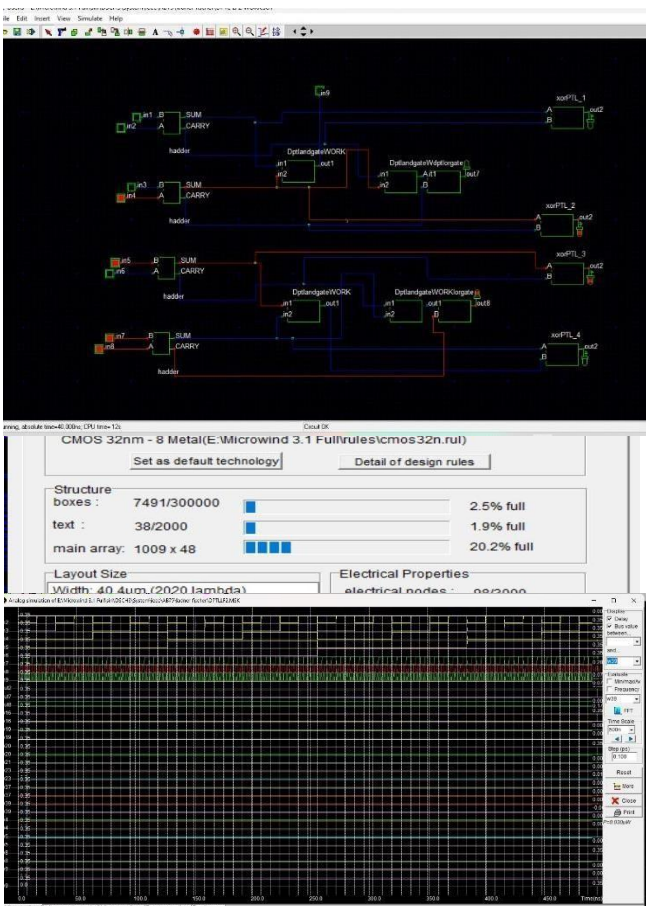


Figure17. execution results of DPTL-based 4-bit Ladner Fischer Adder

To attain results from the design, let us consider the input bits 00, 01, 10, 11, and $C_{in}=0$. It gives the output sum = 0110 and carryout=1110. Microwind3.1 tool is used to obtain the Area and Power results of the 4-bit Ladner Fischer adder using DPTL logic. The Area results are shown in Figure 18.

Figure 18. Area results of DPTL-based parallel prefix Ladner Fischer Adder

If we observe the above figure, we conclude that the Area occupied by 4-bit using DPTL logic Ladner Fischer Adder is given as 592.3 μm^2 . The Power was observed as 0.030um from the design simulation.

Figure 19. simulation results of DPTL-based 4-bit Ladner Fischer Adder RESULTS

S. N O	Parameters	Cmos	Ptl	Dptl
1.	Power	5.12uw	3.925uw	0.030uw
2.	Height	5.7um	5.5um	14.7um
3.	Area(surf)	192.2um	198.1um	592.3um

CONCLUSION

A 4-bit Ladner Fischer adder using CMOS logic, Pass Transistor Logic, and Double Pass Transistor Logic is designed to attain power efficient Ladner Fischer adder. These three designs are constructed and examined from the view of Power. It is concluded that the 4-bit Ladner Fischer adder which is designed by using Double-pass transistor logic gives less power consumption. This proposed double pass transistor

logic used in 4-bit Ladner Fischer Adder is best fitting for many electronic applications such as VLSI and DSP applications. The future aspects depend on the comparison of different parallel prefix adders to tell which one is better to fit in different Electronic Applications.

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