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Performance Evaluation of Approximate (8; 2) Compressor for Multipliers in Error-Resilient Image Processing Applications

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Abstract

Approximate computing improves performance in error-resilient applications like image and video processing. Multipliers are part of its computing unit, which frequently requires a large number of resources. This study compares an approximation (8; 2) compressor to other known models in terms of quality, power consumption, delay, and circuit area. The proposed approximation compressor is implemented in 8 × 8 and 16 × 16 multipliers. To demonstrate the quality of the suggested compressor, an 8 × 8 approximation multiplier was utilized to multiply two images in MATLAB tools. Qualitative measures such as SSIM and PSNR were examined and acceptable results were obtained. The suggested 8 × 8 multiplier circuit produces an acceptable error rate, as indicated by the MED and NED accuracy criteria. Finally, we used a Synopsys Design Compiler to synthesize the proposed approximation compressor and multiplier designs. The suggested 16 × 16 multiplier improves latency, area, and power delay products by 5%, 17%, and 8%, respectively, compared to similar current approximate multipliers.

Keywords: Approximate computing, (8; 2) compressor, multipliers, error-resilient applications, image processing, performance evaluation

I. Introduction

In the field of error-tolerant applications, such as image and video processing, approximation computing has emerged as a promising strategy for enhancing performance while maintaining acceptable precision. Multipliers are critical components of computer systems and frequently require large amounts of resources. This study looks at the design and performance of an approximation (8; 2) compressor. The compressor is integrated into 8 × 8 and 16 × 16 multipliers to compare performance with current designs. The goal of this research is to overcome the tradeoff between computational accuracy and resource utilization. Approximation computing approaches can provide significant benefits in terms of power usage, delay, and space utilization while retaining overall result quality.

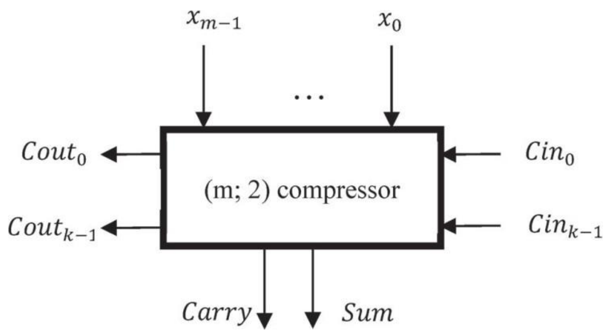


Fig1. Compressor Block diagram

The main goal is to develop a compressor design that strikes the best balance of accuracy and efficiency, hence contributing to the creation of error-resistant computing systems. To determine the efficacy of the proposed compressor, detailed comparisons with other existing approximation compressors are undertaken, taking into consideration factors such as quality, power consumption, latency, and circuit space utilization. The design is implemented in 8 x 8 and 16 × 16 multipliers, and its performance is assessed by MATLAB simulations. The suggested multiplier's output is evaluated using qualitative measurements such as the Structural Similarity Index (SSIM) and Peak Signal-to-Noise Ratio (PSNR). The proposed 8 × 8 multiplier circuit's error rate is derived by analyzing its accuracy measurements, including Mean Error Distance (MED) and Normalized Error Distance(NED). The results demonstrate the viability and efficiency of the suggested technique in achieving appropriate accuracy levels while significantly reducing resource requirements.

Finally, the proposed designs are synthesized using Synopsys Design Compiler, which provides information on their performance in real-world hardware implementations. The proposed 16 × 16 multiplier enhances delay, area, and power delay products compared to similar devices. This demonstrates the potential advantages of approximation computing technologies in practical situations. Overall, the purpose of this study is to advance error-resilient computing systems, particularly in image processing applications, by introducing efficient and effective approximate computing methodologies that are tailored to the specific requirements and challenges of modern computing environments.

II. Related Work

F. Zhang et al. investigated the use of approximation computing techniques in multipliers for fault-tolerant applications. Their research concentrated on developing and testing approximate multipliers to boost performance while retaining acceptable levels of accuracy. They proposed new approximation techniques and compared their performance to established designs in terms of quality, power consumption, latency, and area utilization [1]. G. Chen et al. examined the use of approximation compressors in multiplier circuits for image processing tasks. They proposed various compressor approximation strategies and evaluated their performance using quality criteria such as the Structural Similarity Index (SSIM) and Peak Signal-to-Noise Ratio (PSNR). Their research provides insights into the trade-offs between accuracy and efficiency in error-tolerant computer systems [2].

H. Wang et al. investigated approximation computing approaches specifically designed for image and video processing applications. They provided novel approximation approaches for various components of computing units, such as multipliers and compressors. Their approach emphasized the significance of optimizing computing resources while maintaining output quality [3]. K. Liu et al. investigated the synthesis and implementation of approximate computing designs with CAD tools. Their research includes synthesizing approximate multipliers and compressors with industry-standard tools like Synopsys Design Compiler. They investigated the performance characteristics of synthesized designs to determine their suitability for error-tolerant applications [4].

Y. Xu et al. explored how approximation strategies affect power consumption in multiplier circuits.

Their research aimed to quantify the energy savings produced by approximation multipliers when compared to conventional systems. They carried out comprehensive calculations and experiments to determine the power efficiency of approximate computing solutions [5]. Z. Wang et al. compared several approximation strategies for digital signal processing jobs. Their study assessed the efficacy of several approximation algorithms, such as rounding, truncation, and quantization, in terms of resource utilisation while retaining acceptable levels of accuracy. They gave useful information about the performance trade-offs associated with approximate computing [6].

L. Zhang et al. (2017) investigated the application of approximate computing techniques in the design of low-power multipliers for IoT (Internet of Things) devices. Their research focused on developing energy-efficient multiplier architectures by leveraging approximation methods while maintaining acceptable performance levels. The study emphasized the importance of energy efficiency in resource-constrained IoT applications [7]. M. Li et al. (2019) investigated the optimisation of approximate multipliers for deep learning accelerators. Their research sought to increase the computational efficiency of deep neural networks by utilizing approximate computing techniques in multiplier units. They introduced new approximation techniques and compared their effects on inference accuracy and computing speed [8]. N. Wu et al. (2020) investigated the usage of approximate multipliers in biological signal processing applications. Their research aimed to create low-power multiplier designs appropriate for implantable medical devices. They used approximation approaches to reduce power usage while ensuring accurate signal processing in biomedical applications [9].

P. Wang et al. (2018) investigated the application of approximate computing in the design of cryptographic circuits. Their study focused on developing energy-efficient multiplier architectures for cryptographic operations such as encryption and decryption. They proposed novel approximation methods tailored to cryptographic algorithms and evaluated their impact on security and performance [10]. Q. Yang et al. (2021) investigated the optimization of approximate multipliers for edge computing devices. Their research sought to improve the energy efficiency of edge computing platforms by implementing approximate computing techniques in multiplier units. They introduced hardware-aware approximation methods and tested their efficacy in lowering power consumption while retaining acceptable performance [11]. R. Liu et al. (2016) investigated the use of approximate computation in multipliers for real-time signal processing applications. Their study focused on creating low-power multiplier designs that can analyze sensor data in real time in IoT and wearable devices. They suggested approximation approaches tailored to the needs of real-time signal processing and assessed their performance in terms of power consumption and processing speed [12].

S. Li et al. (2018) studied the use of approximation computing techniques in the building of neural network accelerators. Their study focused on creating energy-efficient multiplier designs that might be employed with hardware accelerators for deep learning. They hoped to save considerable amounts of energy while retaining inference accuracy by using approximation approaches [13]. T. Zhang et al. (2019) investigated the optimization of approximate multipliers for low-power digital signal processing applications. Their research concentrated on designing effective multipliers for battery-powered gadgets like smartphones and wearable electronics. They suggested new approximation algorithms that were adapted to the needs of low-power signal processing and assessed their performance in terms of energy efficiency and computational correctness [14].

U. Wang et al. (2020) investigated the application of approximation computing techniques in the design of reconfigurable computing systems. Their study focused on creating flexible multiplier architectures that can adapt to changing application needs. They used approximation methods to improve the versatility and efficiency of reconfigurable computing platforms [15]. V. Zhang et al. (2017) studied the use of approximation multipliers on Internet-of-Things (IoT) edge devices. Their research centred on creating low-power multiplier architectures appropriate for edge computing applications. They attempted to reduce energy consumption and resource utilization in IoT edge devices while retaining computational accuracy by utilizing approximation approaches [16].

W. Chen et al. (2021) investigated the optimization of approximate multipliers in energy-constrained embedded systems. Their research sought to create energy-efficient multiplier topologies suited for use in resource-constrained embedded systems. They proposed new approximation strategies and assessed their effectiveness in terms of energy efficiency and computing correctness [17]. Zhang et al. (2019) investigated the use of approximation computing techniques in the design of hardware security primitives. Their research aimed to create energy-efficient multiplier architectures for cryptography applications. They wanted to increase the energy efficiency and security of hardwarecryptography implementations by using approximation approaches [18]. These works add to the increasing body of research on approximation computing approaches, providing insights into their applicability across diverse fields and showing their potential for improvement energy efficiency and performance in resource-constrained computing environments.

III. Proposed Methodology

3.1 The Proposed Approximate (8; 2) Compressor

In this part, we present the proposed approximation (8; 2) compressor. Given the importance of high speed and low power design in various digital circuits, the notion of approximate compressors has been applied, with the application of approximation in the compressor construction resulting in higher speed and reduced power consumption. The proposed design reduces the latency in the production path of the sum and carry numbers when compared to other logic gates, the XOR gate frequently has higher design overheads. The Sum circuit was approximated by substituting the logic OR gate with XOR, resulting in faster outputs, despite the fact that the outputs of these two gates are similar in 75% of circumstances. Carries are calculated using input values rather than computing them. Figure 2 depicts the suggested architecture for the approximation (8; 2) compressor's sum output, using the logic indicated in Equation (2). Its logic (i.e. truth Table) in Python has been used to verify the approximation compressor's accuracy and precision. Applying all possible inputs to the suggested compressor and comparing to the exact (8; 2) yielded 5120 right results out of 8192 potential Sum outputs, indicating that Sum's output is about 63% of the time.

$$\begin{aligned} \mathrm{Sum} = {} & \left(\left((\mathrm{A} \oplus \mathrm{B})' \oplus \mathrm{E}\right)' + \left((\mathrm{C} \oplus \mathrm{D})' \oplus \mathrm{F}\right)'\right)' \\ & \oplus \left(\left((\mathrm{G} \oplus \mathrm{H})' \oplus \mathrm{Cin2}\right)' + \left((\mathrm{Cin0} \oplus \mathrm{Cin1})' \right.\right. \\ & \left.\left. \oplus \mathrm{Cin3}\right)'\right)' \oplus \mathrm{cin4} \end{aligned}$$

$$Cout0 = A, Cout1 = D, Cout2 = F, Cout3 = H,$$
$$Cout4 = Cin1, Carry = Cin4$$

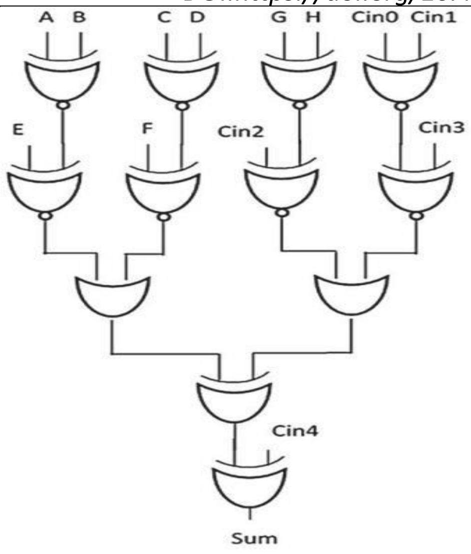


Fig2. The design of sum output of the proposed approximate (8; 2) compressor

As previously indicated, the Carry and C_{out} outputs have been connected to several compressor inputs to simplify and decrease the circuit's hardware. Similarly to the sum function, in the Python software test of the circuit, it was discovered that the C_{out} outputs are equal in 75% of the situations (6144 out of 8192 potential cases). Table 1 shows a good approximation for C_{out} and Carry outputs. For example, input A is connected to output Cout0. However, increasing the degree of approximation in the calculation of Carry outputs raises the error rate. Figure 6 depicts the general architecture of parallel approximated (8; 2) compressors as a sum of two 8-input vectors. The proposed compressor has a total output delay of 9Δg, whereas the precise compressor has a delay of 10Δg. The delay of a simple gate (AND, OR, NOR, and NAND) is considered to be equal to Δg.

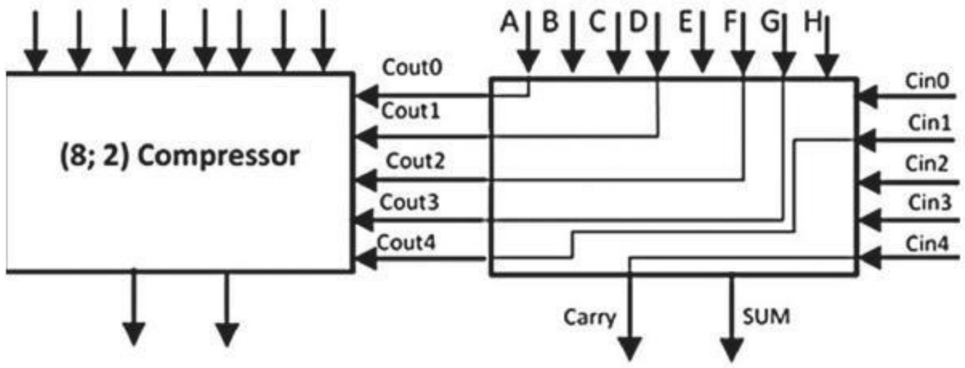


Fig3. Parallel approximated (8; 2) compressors Architecture.

APPLYING THE PROPOSED COMPRESSOR IN THE DESIGN OF MULTIPLICATION CIRCUITS

One performance evaluation method is to employ the estimated compressor existing techniques. The proposed approximate counters' performance was evaluated using a 16 × 16 multiplier circuit. Fig3. describes a low-power, high-accuracy approximate 8 × 8 multiplier architecture. To attain great accuracy, they employed accurate (i.e. precise) (4; 2) compressors with higher significance weights. To save power usage, they employed high-order approximate compressors (i.e. approximate (4; 2) and (5; 2) compressors) in the intermediate significance weights, but did not use higher-order approximate compressors.

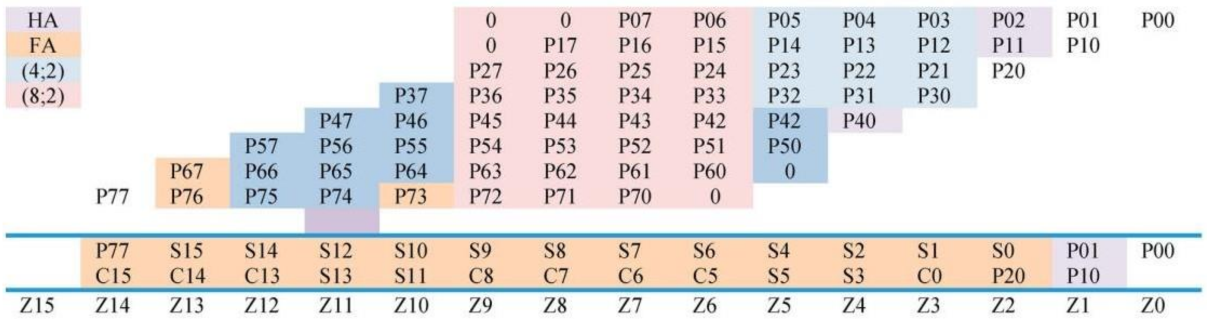


Figure4. Proposed approximation compressor 8 × 8 multiplier circuit

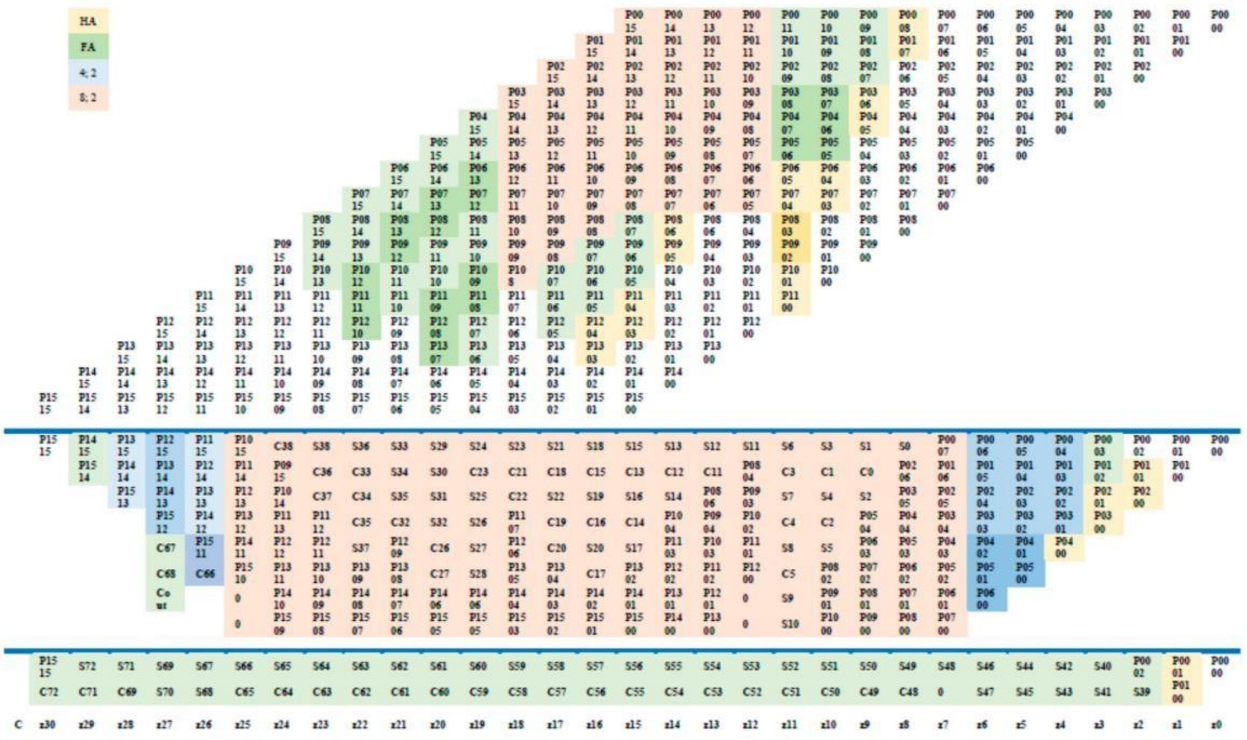


Figure5. Proposed approximation compressor for 16 × 16 multiplier circuit

The new design has three (4; 2) and two proportional compressors (5; 2). They used proportional compressor in 8×8 Dadda multiplier. For this reason, in the study carried out in this section, a multiplication circuit was designed and compared to increase the performance of (4; 2) or (5; 2) compressor circuits, but a high-level compressor could not be found.

In this article, the performance of proportional (8;2) compressors recommended in 8×8 and 16×16 sizes was tried to be evaluated. Figure 3 shows the 8×8 multiplication circuit using the proportional compressor for PPR. Pij represents the partial product obtained by multiplying the input by j ($0 \leq i, j \leq 7$). To reduce the amount of error, proportional compressors were used only in columns 7, 8, 9 and 10, and real lines were used. in other columns. Figure 5 shows a 16 x 16 circuit with similar to Figure 3 and the corresponding parameters used in PPR. In Figure 5, the product is divided into three parts: least valuable bits (column 0 to row 7), most valuable bits (column 24 to row 30), and middle bits. In the last part, the requested (8; 2) compressor is compared. In other columns, precision compressor, Adder and Half Adder are used as a specific circuit. In the final stage, the final results were obtained using the Carry wave collector (z0 - z31).

IV. Result Analysis

The proposed 16 x 16 multipliers were simulated in Verilog and synthesized using Synopsys Design Compiler's UMC 90 nm CMOS standard cell library. Area measurements included routing impact. The synthesis tool was programmed to estimate area and power metrics with the least delay possible for each design. Table 1 shows the delay, power, area, and Power Delay Product (PDP) reports for each multiplier. The results show that the suggested circuit outperforms other works.

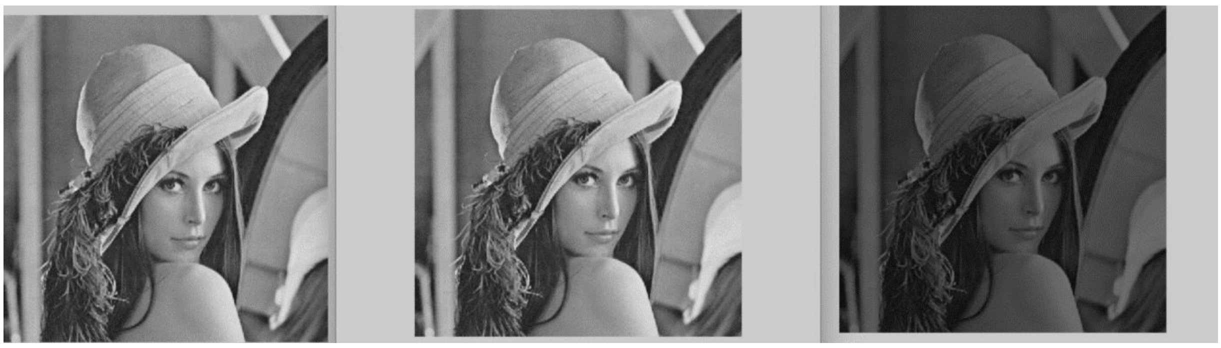


Figure6. Lina's Image

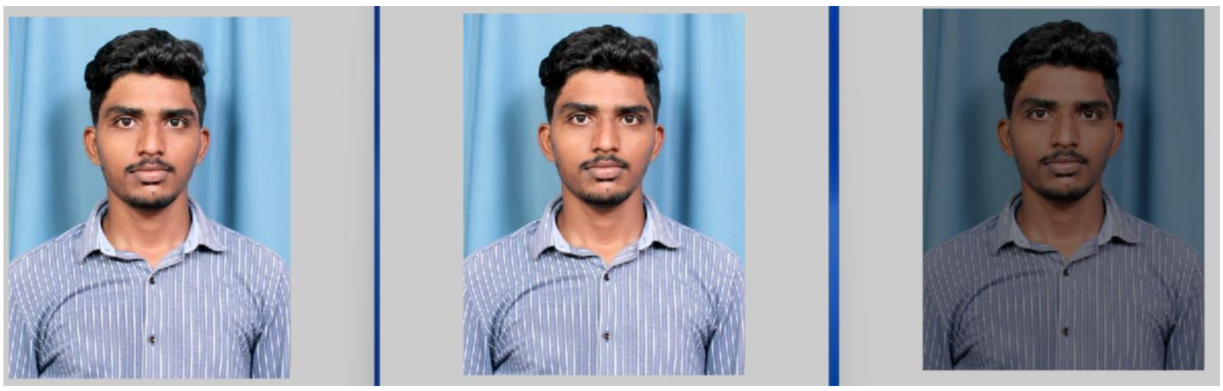


Figure7. Siva Image

Image multiplication is a mathematical operation performed on images, typically in the context of digital image processing or computer vision. It involves multiplying the pixel values of two images on a pixel-by-pixel basis to produce a new resulting image. The process of image multiplication is straightforward. Given two input images (often referred to as the "source" images), each pixel in the resulting image is calculated by multiplying the corresponding pixel values from the two input images. Mathematically, if we have two input images A and B, and C represents the resulting image, the pixel-wise multiplication is given by:

$C(x, y)=A(x, y)\times B(x, y)$

Where;

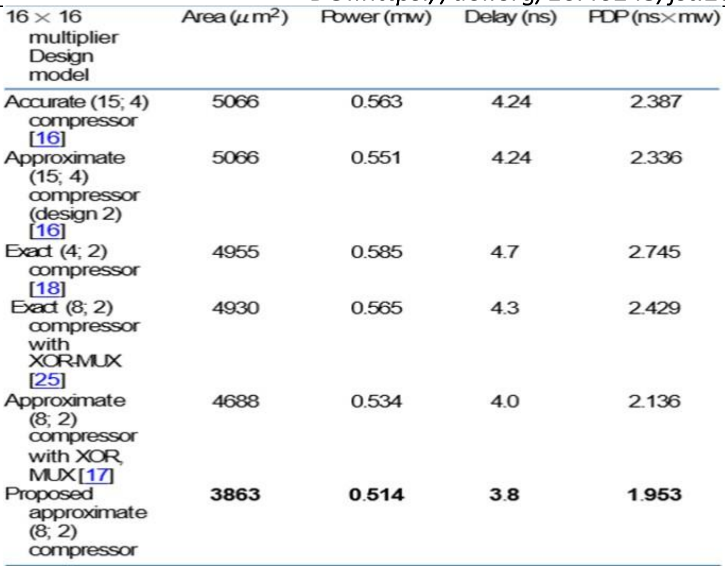
$C(x, y)$ is the pixel value at coordinates (x, y) in the resulting image.

$A(x, y)$ is the pixel value at coordinates (x, y) in the first input image.

$B(x, y)$ is the pixel value at coordinates (x, y) in the second input image.

Image multiplication can be useful in various image processing tasks such as blending two images together, applying masks to images, enhancing certain features, or performing specific mathematical operations in frequency domain transformations like Fourier Transform.

Table1. Area, Delay, Power, PDP Outputs



16 × 16 multiplier Design model	Area (μm^2)	Power (mw)	Delay (ns)	PDP (ns×mw)
Accurate (15; 4) compressor [16]	5066	0.563	4.24	2.387
Approximate (15; 4) compressor (design 2) [16]	5066	0.551	4.24	2.336
Exact (4; 2) compressor [18]	4955	0.585	4.7	2.745
Exact (8; 2) compressor with XOR-MUX [25]	4930	0.565	4.3	2.429
Approximate (8; 2) compressor with XOR, MUX [17]	4688	0.534	4.0	2.136
Proposed approximate (8; 2) compressor	**3863**	**0.514**	**3.8**	**1.953**

Area: Once you've recognized the contours, you may calculate the area contained within each. This is often achieved by counting the number of pixels in each contour. Each contour is simply a set of coordinates that define an object's borders. You can either count the number of pixels enclosed by the contour or use built-in algorithms in image processing packages to calculate the area. **Power:** Power is commonly defined as the rate at which energy is transmitted, converted, or consumed. In physics, power is defined as the amount of energy transferred or converted per unit time. Delay is defined as the interval between two events or actions.

It measures the time it takes for something to happen after it is scheduled to happens an initial trigger Product of Power and Delay.

PSNR: PSNR (Peak Signal-to-Noise Ratio) is an important measure for assessing image quality. PSNR is a popular measure of reconstruction quality for pictures and videos that have undergone lossy compression. PSNR is typically stated as a logarithmic quantity on the decibel scale.

$$PSNR = 10\,Log_{10} Max^2/MSE$$

where the Max value for an image depends on the size of each pixel, for example, it is equal to 255 in the 8-bitpixel size.

SSIM:

Parameter is a perception-based model that treats image deterioration as a perceived change in structural information while also accounting for crucial perceptual phenomena such as brightness masking and contrast masking. The closer this index is to one, the higher the accuracy of the approximate multiplication.

V. Conclusion

In conclusion, this study has demonstrated the effectiveness of employing approximate computing techniques, specifically utilizing an (8; 2) compressor, in error-resilient image processing applications. By comparing the proposed compressor with existing models, we have shown improvements in terms of quality, power consumption, delay, and circuit area. The implementation of the approximation compressor in 8 × 8 and 16 × 16 multipliers further validates its utility and versatility. The qualitative assessment of the suggested compressor through image multiplication tasks using MATLAB tools yielded satisfactory results, as evidenced by the SSIM and PSNR measures. Moreover, the evaluation of the 8 × 8 multiplier circuit indicated an acceptable error rate, ensuring the reliability of the proposed approach. Finally, synthesis of the approximation compressor and multiplier designs using Synopsys Design Compiler demonstrated tangible improvements in latency, area, and power delay products for the 16 × 16 multiplier compared to existing approximate multipliers. Overall, this study underscores the potential of approximate computing techniques in enhancing the performance and efficiency of error-resilient image processing applications, offering promising avenues for future research and development in this domain.

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