Journal of Science and Technology
ISSN: 2456-5660 Volume 8, Issue 1 (January2023)
www.jst.org.in *DOI:https://doi.org/10.46243/jst.2023.v8.i01.pp06-18*

AN STRATEGY OF POWER AND AREA COMPETENT APPROXIMATE MULTIPLIERS

[1] CHINTHALA KAVYA, [2]MOHAMMAD GANDHI BABU,[3]DR. N. SURESH

[1]PG SCHOLAR, [2]ASST. PROFESSOR, [3]ASSOSCIATE PROFESSOR & HOD

DEPARTMENT OF ECE, AVN INSTITUTE OF ENGINEERING AND TECHNOLOGY, M, KOHEDA ROAD, M.P. PATELGUDA POST IBRAHIMPATNAM, DIST, HYDERABAD, TELANGANA 501510.

To Cite this Article

CHINTHALA KAVYA, MOHAMMAD GANDHI BABU,DR. N. SURESH **‘‘„AN STRATEGY OF POWER AND AREA COMPETENT APPROXIMATE MULTIPLIERS„** *’’, Journal of Science and Technology, Vol. 08, Issue 1-January 2023, pp06-18*

Article Info

Received: 19-12-2022 *Revised: 8-01-2023* *Accepted: 17-01-2023* *Published: 27-01-2023*

ABSTRACT:

In this paper, the area of efficiency multiplier put a sign suggests a fixed width through a replica redundancy through adoption My tolerance for noise (ANT) architecture with a multiplier of fixed width to build a redundancy version precision cutting Masa (RPR). ANT proposed architecture can meet the demand for high precision, low power consumption, and region Efficiency. RPR fixed-width design with error compensation through the circles of the possibilities and statistical analysis. use the When a partial product of the correct input vectors and vectors fixed in the palace and put in place to reduce truncation errors, hardware Failure holding circuit can be simplified compensation. The multiplier ANT 16 × 16 bits, the circuit area in our RPR fixed width It may be less, energy consumption in the design of ants can be saved as compared with the ANT state of the art design.

Keywords: Algorithmic Noise Tolerant (ANT), Fixed-Width Multiplier, Reduced-Precision Replica (RPR), Voltage Over Scaling (VOS), Error Tolerant Adder(ETA),Main Digital Signal Processing(MDSP)

INTRODUCTION:

The rapid growth of mobile and wireless systems In recent years, the need for systems pushing ultra-low energy. To reduce power dissipation, and measuring the voltage. [1] It is widely used as a technology of low energy efficient, and Power consumption in CMOS circuits game The square of the supply voltage. However, in the semi-depth micrometer process technologies, has raised the problems of noise interference Difficulty in design and efficient reliable microelectronic Systems, and therefore, design techniques to improve the noise Tolerance has developed a large scale [2] - [8]. Aggressive low energy technology, referred to as the voltage across the dimensioning (VOS), and aim to reduce the supply volt age out critical supply voltage without sacrificing productivity. However, VOS lead to a sharp deterioration in the signal to noise ratio, Ratio (SNR). My novel noise tolerant (ANT) The combination of technology VOS main block with low resolution Copy (RPR), who is struggling with software bugs effectively, while Achieve significant energy savings. Some ANT deformation The designs presented in [5] - [9] The design concept is ANT Extended system level. However, the design of RPR ANT is intended, and that is not easy Adopted and repeatedly. RPR designs in ANT designs can work on Too fast, but the hardware complexity is also Complex as shown in Figure 1. As a result, the design RPR ANT design design is still the most popular because of its Simplicity. However, with the adoption of RPR must still pay In the additional area and power consumption. In this work, We also suggest an easy way by using a fixed-width RPR To replace the block RPR full width. The use of a fixed width RPR, a miscalculation can be corrected with low Energy consumption and low overhead region. we use Probability and statistics, and a partial analysis of the product weight Finding a company about compensation for greater accuracy RPR design. In order not to increase the critical path delay, Restricting compensation circuit in the RPR should not be Located on the critical path. As a result, we can achieve ANT is designed with the small area of the circle, low power Consumption, supply voltage and less critical

ANT multiplier design proposed US-ING A fixed-width RPR

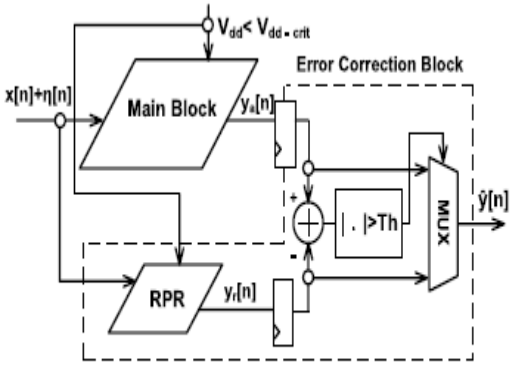

Fig. 1. ANT architecture [2].

In this paper, we have proposed, and the width RPR-fixed Rip place a total width of blocks RPR ANT design [2], It is shown in Figure 2, which can not only provide the highest Account

accuracy, low power consumption, low Above the area of the RPR, but also carried out with high SNR, The effective area and the tension of the lower layer sup operation and low power consumption to achieve more ANT architecture. We demonstrate our wide design based on RPR fixed ANT ANT multiplier. Constant width designs usually DSP applications applied to prevent the growth of countless littleTo show. Court n bits least significant bit (LSB) output is popular solution for the construction of a fixed width with n bits DSP The inputs and outputs n bits. Hardware complexity and power DSP consumption of a fixed width is usually about half One full length. However,truncated LSB results pane In rounding error, you need to compensate specifically. Many of Arts offer to reduce truncation Error correction with the value of continuing with the correct variable Value. The complexity of the circuit to compensate for a fixed The corrected value can be simpler than the variable Correction value. However, approaching the correct variable Usually more accurate, method of compensation is truncation error compensation between longitudinally Multiplier and fixed-width multiplier. However, in RPR has a fixed width of the multiplier ANT, compensation A mistake we have to correct is the general truncation error MSDP mass. On the contrary, we have a method of compensation for truncation error compensation between longitudinally MSDP multiplier and fixed-width multiplier RPR. Currently, there are a lot of fixed width multiplier Designs applied to the complications of full width. However, there It is not yet fixed width design RPR applied to the ANT multiplexed designs. To achieve more accurate Error Compensation, which offset truncation error with variable correction value. Error building compensation circuit especially the use of terms of partial products With more weight in less than a big slice. The The algorithm error compensation benefits from the possibility, Statistics, linear regression analysis to find The approximate amount of compensation [16]. To save the hardware Complexity, partial compensation carriers Product What has the greatest weight in less than a big slice And it is injected directly into the fixed RPR offer, which does not Need more logic gates compensation [17]. For more

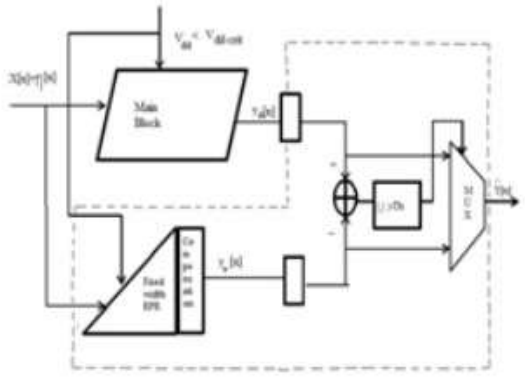

Fig.2. Proposed ANT Architecture with fixed width RPR.

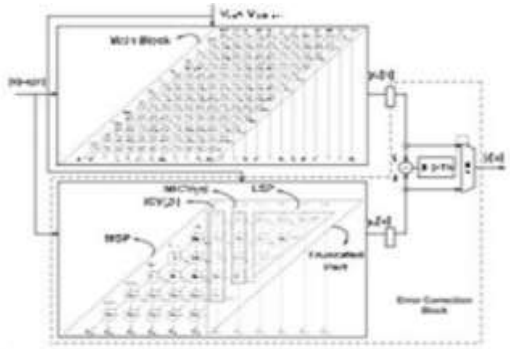

Fig.3.16 × 16 bit ANT multiplier is implemented with the 8-bit fixed width Replica redundancy block.

with less Error compensation, but must also take into account the impact of Truncated with the second most important bits products Error compensation. We propose a compensation error Circuit using the simple vector corrected minor tickets He remained offset error. In order not to increase critical path delay, and we are in a position Compensation Service in noncritical path of RPR fixed width. Compared to RPR complete design introduced in [15] and proposed a fixed width RPR multiplier leads not only with high SNR but also Circuits with low area and low power consumption. An error in the static screen proposed correction vector minutes ANT design highlighted in the design, function RPR To correct the errors that occur at the start and MSDP Maintaining the SNR of the entire system during cutting supplies Aalkahrby effort. If a fixed-width RPR is used to ANT Architecture, and it went for a smaller circuit area and power Consumption, but also accelerate the speed of calculation, Compared to traditional total length of the RPR. But nevertheless, We need huge compensation truncation error due to cut Stop many hardware elements of the MSDP LSB. At MSDP n bits ANT POV-multiplier and the Crown

group, two for And it can be expressed in a signed n-bit input X and Y as he (/ 2 N) all Baugh-bit width and partial Crown unsigned product Group can be divided into four sub-groups, which are the most A large part (MSP), correct input vector [ICV (SS)].

Fault tolerant application ADDER

In digital signal processing In photos and many other DSP processing applications, Fast Fourier Transform (FFT) is very important Function. FFT calculation involves a A number of additions and strokes. It is therefore A good platform to include our pro-ETA raised. to try Viability of ETA, which put all the common Extras involved in the normal track algorithm with our French Federation It was suggested that the account is added. As we all know, the digital image Represented by the matrix in the DSP system, each element Matrix represents the color of a single pixel of the image. To compare the quality of the images and processed by each of the Traditional French Federation French Tennis Federation minutes of tennis, which housed ETA have proposed, we have created the following Experience. The image has been translated for the first time in the form of a matrix It is sent through the standard system that made use of the usual French Tennis Federation and the French Union of reverse normal tennis. This output matrix The system then turned back to the image and the screen In Figure 3. It was also treated the same image matrix in FFT system used accurate and inaccurate vice FFT, where both 16-bit multiplier FFT include It is described in section, with the image processed form. 4 (b). Although the two matrices derived from the same image They are different, and the two images that have been obtained (see Figure 4) are Often the same thing. Figure 4 (b) is a little darker and has a horizontal bands of different shades of gray Implementation of multiplier contains three steps: era of partial merchandise, partial products reduce charge tree, and ultimately, a vector merge addition to deliver final product from the sum and convey rows generated from the reduction tree. Second step consumes greater energy. In this short, approximation is carried out in discount tree degree.

Implementation of multiplier contains three steps:

- Generation of partial merchandise,
- Partial products bargain tree, and in the end,

- a vector merge addition to deliver very last product from the sum and produce rows generated from the cut price tree.

Second step consumes extra energy. In this brief, approximation is executed in bargain tree diploma. A 8-bit unsigned1 multiplier is used for example to provide an cause of the proposed approach in approximation of multipliers. Consider 8-bitunsigned enter operands α = _7m=0 αm2m and β = _7n=0 βn2n.

The partial product am,n = αm ⋅ βn in Fig 1. is the end result of AND operation many of the bits of αm and βn.The proposed approximate approach may be performed to signed multiplication which includes Booth multipliers as well, besides it is not executed to signal extension bits.

Fig. 1. Transformation of generated partial products into altered partial products.

From statistical point of view, the partial product am,n has a probability of 1/4 of being 1. In the columns containing more than three partial products, the partial products am,n and an,m are combined to form propogate and generate signals as given in (1). The resulting propogate and generate signals form altered partial products pm,n and gm,n. From column 3 with weight 23 to column 11 with weight 211, the partial products am,n and an,m are replaced by altered partial products pm,n and gm,n. The original and transformed partial product matrices are shown in Fig. 1

$p_{m,n} = a_{m,n} + a_{n,m}$

$g_{m,n} = a_{m,n} \cdot a_{n,m}$. (1)

The probability of the altered partial product gm,n being one is 1/16, which is significantly lower than 1/4 of am,n. The probability of altered partial product pm,n being one is 1/16 + 3/16 + 3/16 = 7/16, which is higher than gm,n. These factors are considered, while applying approximation to the altered partial product matrix.

Approximation of Altered Partial Products g(m,n):

The accumulation of generate signs is completed column realistic. As every element has a danger of one/16 of being one, elements being 1 inside the same column even decreases. For example, in a column with four generate indicators, opportunity of all numbers being 0 is (1 − pr)four, only one element being one is 4pr(1 − pr)3, the possibility of factors being one within the column is 6pr2(1 − pr)2, 3 ones is 4pr3(1−pr) and threat of all elements being 1 is pr4, in which pr is 1/16. The opportunity statistics for a number of generate elements m in each column are given in Table I. Based on Table I, using OR gate inside the accumulation of column smart generate elements in the altered partial product matrix gives precise result in most of the instances. The opportunity of errors (Perr) at the same time as the usage of OR gate for cut price of generate indicators in every column is likewise indexed in Table I. As can be seen, the risk of mis prediction might be very low. As the number of generate alerts will increase, the error possibility increases linearly. However, the fee of blunders also rises. To prevent this, the maximum sort of generate indicators to be grouped with the aid of OR gate is saved at four. For a column having m generate signals, m/4 OR gates are used.

Approximation of Other Partial Products:

The accumulation of different partial merchandise with danger ¼ for am,n and seven/16 for pm,n uses approximate circuits. Approximate half-adder, complete-adder, and 4-2 compressor are proposed for his or her accumulation. Carr y and Sum are two outputs of those approximate circuits. Since Carr y has better weight of binary bit, mistakes in Carry bit will contribute greater through generating errors difference of in the output. Approximation is handled in this kind of way that absolutely the distinction between real output and approximate output is constantly maintained as one. Hence Carr y outputs are approximated most effective for the instances, wherein Sum is approximated. In adders and compressors, XOR gates have a propensity to make contributions to excessive location and postpone. For approximating half-adder, XOR gate of Sum is modified with OR gate as given in (2). This effects in one mistakes inside the Sum computation as visible in the reality desk of approximate 1/2-adder in Table II. A tick mark denotes that approximate output suits with accurate output and circulate mark denotes mismatch

Sum = x1 + x2

Carr y = x1 ・ x2.(2)

In t he approximation of full-adder, one of the two XOR gates is replaced with OR gate in Sum calculation. This results in error in last two cases out of eight cases. Carr y is modified as in (3) introducing one error. This provides more simplification, while maintaining the difference between original and approximate value as one. The truth table of approximate full-adder is given in Table III

W = (x1 + x2)

Sum = W ⊕ x3

Carr y = W ・ x3.(3)

Two approximate 4-2 compressors in [5] produce nonzero output even for the cases where all inputs are zero. This results in high ED and high degree of precision loss especially in cases of zeros in all bits or in most significant parts of the reduction tree. The proposed 4-2 compressor overcomes this drawback. In 4-2 compressor, three bits are required for the output only when all the four inputs are 1, which happens only once out of 16 cases. This property is taken to eliminate one of the three output bits in 4-2 compressor.

TRUTH TABLE OF APPROXIMATE HALF ADDER

TABLE II

Inputs		Exact outputs		Approximate outputs		Absolute Difference
x1	x2	carry	sum	carry	sum	
0	0	0	0	0	0	0
0	1	0	1	0	1	0
1	0	0	1	0	1	0
1	1	1	0	1	1	1

TRUTH TABLE OF APPROXIMATE FULL ADDER

To maintain minimal error difference as one, the output “100" (the value of 4) for four inputs being one has to b replaced with outputs “11" (the value of 3). For Sum computation, one out of three XOR gates is replaced with OR gate. Also, to make the Sum corresponding to the case where all inputs are ones as one, an additional circuit x1 ・ x2 ・ x3 ・ x4 is added to the Sum expression. This results in error in five out of 16 cases. Carr y is simplified as

in (4). The corresponding truth table is given in Table IV

W1 = x1 ・ x2

W2 = x3 ・ x4 Sum = (x1 ⊕x2) + (x3 ⊕x4) + W1 ・ W2

Carr y = W1 + W2. (4)

Fig. 2 shows the reduction of altered partial product matrix of 8*8 approximate multiplier. It requires two stages to produce sum and carry outputs for vector merge addition step. Four 2-input OR gates, four 3-input OR gates, and one 4-input OR gates are required for the reduction of generate signals from columns 3 to 11. The resultant signals of OR gates are labeled as Gi

corresponding to the column i with weight 2i . For reducing other partial products, 3 approximate half-adders, 3 approximate full-adders, and 3 approximate compressors are required in the first stage to produce Sum and Carr y signals, Si and Ci corresponding to column i . The elements in the second stage are reduced using 1 approximate half-adder and 11 approximate full-adders producing final two operands xi and yi to be fed to ripple carry adder for the final computation of the result.

TABLE III

INPUT			Exact Output		Approximation output		Absolute Difference
x1	x2	x3	carry	sum	carry	sum	
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	1	0	1	0
0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	0
1	0	1	1	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	1	1	1	0	1

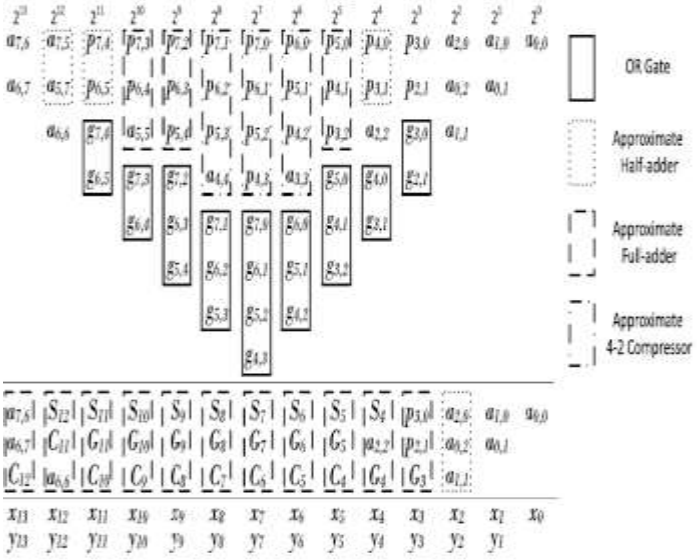

Fig. 2. Reduction of altered partial products.

IMAGE PROCESSING

Geometric imply filter is broadly utilized in picture processing to lessen Gaussian noise [13]. The geometric mean filter out is higher at maintaining aspect capabilities than the arithmetic suggest clear out. Two sixteen- bits in keeping with pixel grey scale images with Gaussian noise are considered. Three × 3 advise filter is used, wherein every pixel of noisy photograph is modified with geometric mean of 3×3 block of neighboring pixels centered round it. The algorithms are coded and carried out in MATLAB. Exact and approximate sixteen-bit multipliers are used to perform multiplication among sixteen-bit pixels. PSNR is used as figure of gain to assess the exceptional of approximate multipliers. PSNR is based totally on suggest-square errors discovered between resulting picture of actual multiplier and the pix generated from approximate multipliers. Energy required by using the use of actual and approximate multiplication way on

the equal time as appearing geometric suggest filtering of the pictures is placed the usage of Synopsys Primetime. Further, real multiplier is voltage scaled from 1 to 0.Eighty five V (VOS), and its impact on energy intake and picture brilliant is computed.

The noisy input photo and resultant photo after denoising the use of true and approximate multipliers, with their respective PSNRs and electricity financial savings in μJ are established in Figs. Four and five, respectively. Energy required for actual multiplication technique for photograph-1 and photo-2 is 3.24 and a pair of.Sixty two μJ , respectively. Although ACM1 has better strength financial savings in comparison to Multiplier1, Multiplier1 has appreciably better PSNR than ACM1. Multiplier2 suggests the quality PSNR amongst all the approximate designs. Multiplier2 has better electricity financial savings, in comparison to ACM2, PPP, SSM, UDM, and VOS. The intensity of photograph-1 being mostly on the lower prevent of the histogram causes horrible usual performance of ACM multipliers. As the switching activity affects maximum tremendous a part of the layout in VOS, PSNR values are affected of advantage to assess the exceptional of approximate multipliers. PSNR is primarily based totally on propose-rectangular mistakes discovered between ensuing picture of proper multiplier and the snap shots generated from approximate multipliers. Energy required via real and approximate multiplication approach at the same time as appearing geometric advocate filtering of the images is found the usage of Synopsys Primetime. Further, real multiplier is voltage scaled from 1 to 0.Eighty 5 V (VOS), and its effect on strength consumption and picture high-quality is computed.

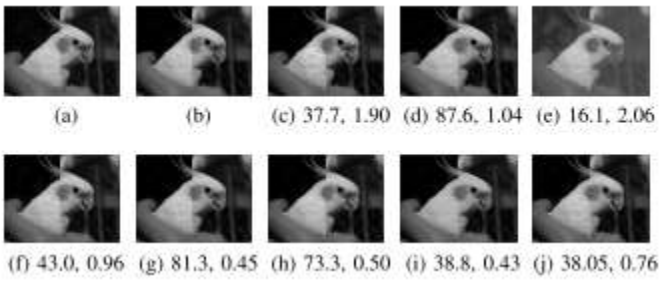

Fig. 4. (a) Input image-1 with Gaussian noise. Geometric mean filtered images and corresponding PSNR and energy savings in μJ using (b) exact multiplier, (c) Multiplier1, (d) Multiplier2, (e) ACM1, (f) ACM2, (g) SSM, (h) PPP, (i) UDM, and (j) VOS.

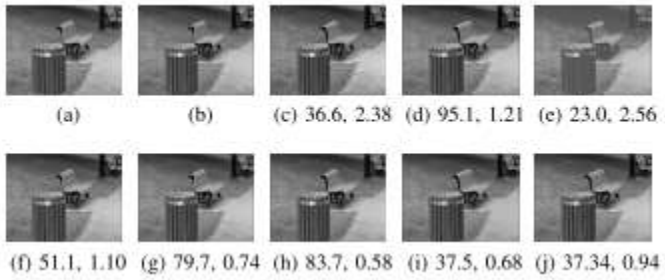

Fig. 5. (a) Input image-2 with Gaussian noise. Geometric mean filtered images and corresponding PSNR and energy savings in µJ using (b) exact multiplier, (c) Multiplier1, (d) Multiplier2, (e) ACM1, (f) ACM2, (g) SSM, (h) PPP, (i) UDM, and (j) VOS.

The noisy enter photograph and resultant photo after denoising the usage of particular and approximate multipliers, with their respective PSNRs and energy financial financial savings in µJ are shown in Figs. 4 and five, respectively. Energy required for exact multiplication approach for photo-1 and image-2 is 3.24 and more than one.Sixty two µJ , respectively. Although ACM1 has higher energy savings compared to Multiplier1, Multiplier1 has notably higher PSNR than ACM1. Multiplier2 shows the first-rate PSNR amongst all the approximate designs. Multiplier2 has better strength financial savings, in contrast to ACM2, PPP, SSM, UDM, and VOS. The intensity of photograph-1 being totally on the decrease surrender of the histogram reasons terrible overall performance of ACM multipliers. As the switching pastime impacts maximum considerable part of the design in VOS, PSNR values are affected.

CONCLUSION

In this paper, it is to introduce the concept of tolerance in error VLSI design. A new species of snake, and the snake error tolerant, That sells a certain amount of Milan-pastor of the importance of Save energy and improve performance, and propose. Wide comparisons with conventional digital hoses It was shown that the proposed multiplier exceeded Traditional power consumption and speed snakes Performance. Potential applications for the fall of the multiplier Especially in areas where there are no strict requirements Accuracy or where ultra-low power consumption and high speed Accuracy is more important than performance. One An example of these applications in the application of DSP portable devices such as mobile phones and laptops.

REFERENCES

[1]B. Melvin, "Let's think analog," in Proc. IEEE Com-put. Soc. Annu.Symp. VLSI, 2005, pp. 2–5.

[2]International Technology Roadmap for Semiconductors [Online].Available: http://public.itrs.net.

[3]B. Melvin and Z. Haiyang, "Error-tolerance and multimedia,"in Proc. 2006 Int. Conf. Intell. Inf. Hiding and Multimedia SignalProcess., 2006, pp. 521–524.

[4]M. A. Breuer, S. K. Gupta, and T. M. Mak, "Design and error tolerancein the presence of massive numbers of defects," IEEE Des. TestComput., vol. 24, no. 3, pp. 216– 227, May-Jun. 2004.

[5]M. A. Breuer, "Intelligible test techniques to sup-port error-tolerance,"in Proc. Asian Test Symp., Nov. 2004, pp. 386–393.

[6]K. J. Lee, T. Y. Hsieh, and M. A. Breuer, "A novel testing methodologybased on error-rate to support errortolerance," in Proc. Int. Test Conf.,2005, pp. 1136–1144.

[7]S. Chong and A. Ortega, "Hardware testing for error tolerant multimediacompression based on linear transforms," in Proc. Defect andFault Tolerance in VLSI Syst. Symp., 2005, pp. 523–531.

[8]H. Chung and A. Ortega, "Analysis and testing for error tolerant motionestimation," in Proc. Defect and Fault Tolerance in VLSI Syst. Symp.,2005, pp. 514–522.

[9]H. H. Kuok, "Audio recording apparatus using an imperfect memorycircuit," U.S. Patent 5 414 758, May 9, 1995.

[10]T. Y. Hsieh, K. J. Lee, and M. A. Breuer, "Reduction of detected acceptablefaults for yield improvement via errortolerance," in Proc.Des., Automation and Test Eur. Conf. Exhib., 2007, pp. 1–6.

[11]V. Palem, "Energy aware computing through probabilisticswitching: A study of limits," IEEE Trans. Comput., vol. 54, no. 9, pp.1123–1137, Sep. 2005.

[12]S. Cheemalavagu, P. Korkmaz, and K. V. Palem"Ultra low energycomputing via probabilistic algorithms and devices: CMOS deviceprimitives and the energy-probability relationship," in Proc. 2004 Int.Conf. Solid State Devices and Materials, Tokyo, Japan, Sep. 2004, pp.402–403.

[13]P. Korkmaz, B. E. S. Akgul, K. V. Palem, and L. N. Chakrapani, "Advocatingnoise as an agent forultra-low energy computing: Probabilisticcomplementary metal-oxidesemiconductor devices and their characteristics,"Jpn. J. Appl. Phys., vol. 45, no. 4B, pp. 3307–3316, 2006.
[14]E. Stine, C. R. Babb, and V. B. Dave, "Constant addition utilizingflagged prefix structures," in Proc.IEEE Int. Symp. Circuits and Systems(ISCAS), 2005.

[15]L.-D. Van and C.-C. Yang, "Generalized low-error areaefficient fixedwidthmultipliers," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 25,no. 8, pp. 1608–1619, Aug. 2005.

[16]Lehman and N. Burla, "Skip techniques for high-speed carry propagationin binary arithmetic units," IRE Trans. Electron. Comput., vol.EC-10, pp. 691–698, Dec. 1962.

[17]O. Bedrij, "Carry select adder," IRE Trans. Electron. Comput., vol.EC-11, pp. 340–346, 1962.

[18]O. MacSorley, "High speed arithmetic in binary computers," IRE Proc.,vol. 49, pp. 67–91, 1961.

[19]Y. KiatSeng and R. Kaushik, Low-Voltage, Low-Power VLSI Subsystems. New York: McGraw-Hill, 2005.